Volume production proven advanced nanometer slurries for CMP applications, capable of recycling and extendable to larger Si wafer sizes and future IC technology nodes

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Biography

Raymond Jin was a Ph.D. graduate with honor from University of Utah in 1988. He has 15 years of industrial experience as a technologist and technical executive in oxide-CMP/STI-CMP/polysilicon-CMP/Si-CMP/low-k-dielectric-CMP/W-CMP/Cu-CMP, material/chemistry R&D, and 0.5um/0.35um/0.25um/0.18um/0.13um/90nm/65nm/45nm FEOL/BEOL process development/integration/technology transferring. He was credited for a leadership role in improving IC device yield by >30% in two different IC fabs. He worked at leading Semiconductor companies, including Applied Materials and National Semiconductor. He introduced CMP to colloidal scientists in a leading Chinese university that later led to the 1st CMP Ph.D. graduated in China. He is currently President and CTO of Adcon Lab, Inc., a global provider of CMP/cleaning solutions, including the broadest standard and application-specific test wafers and IC fab services, a technology developer and manufacturer of the world-1st commercially available nanometer ceria suspensions for CMP: NanoCeria™ product. Over last three years, he has led his company in developing CMP R&D, manufacturing, sales/marketing, and customer support organizations at three major industry centers in China. He has 33 technical publications and several patents issued and filed.

Xiaolan Song was a M.S. graduate in materials science from Wuhan University of Technology in 1987. She joined Adcon Lab, Inc. in 2001 and managed several CMP projects in China. Currently she is a senior CMP engineer and project manager at Adcon.

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Abstract

This paper reports CMP technology break-through in designing and commercializing the size-distribution-controlled nanometer slurries manufactured at semiconductor-manufacturing site, capable of recycling in volume production setting and extendable to larger Si wafer sizes and future IC technology nodes.

New nanometer slurries proved during a >3000-wafer continued run that >50% CoO/CoC reduction was achieved by using the 1st-ever locally manufactured CMP slurry in China and recycling the slurry during Si wafer production, thus minimizing shipping cost and reducing slurry consumption by orders of magnitudes. Furthermore, higher environmental standard was enforced by slurry recycling.

By controlling the nanometer abrasive particle size distribution, abrasive particle composition, solution chemistry, rheological and tribological properties, and surface and interfacial properties of abrasive particulates and the materials being polished away during the manufacturing processes, new slurries based on highly concentrated components from oversea and bulky portion of the components in slurry manufactured in China were able to demonstrate long stability and superior polishing performance (as manifested by high planarity, low defects and higher yield) over a >3000-wafer continued production run as compared to the baseline over several years of production run.

Introduction

In a typical semiconductor fab today, CMP slurry expenses have accounted for nearly one third of total cost of ownership (CoO) in entire CMP operation (including CMP manufacturing equipment and CMP consumables). To be manufacturing technology leader and achieve business success in fast-paced IC device technology advancement, CMP engineers and fab operation executives have to constantly look for and implement the new slurries and other CMP consumables (including pad, conditioning disk, and retaining ring) on their CMP systems that enable more advanced IC technology by improved CMP performance and thus lower CMP operation cost in their own fab. [1-13]

Nanometer silica abrasives, various chemistries, and process technologies have been used in new slurry for improved CMP performance in volume production in the past. This paper reports the advancement of new technologies in the semiconductor volume production for standard revenue product in a semiconductor fab. The new technologies reported in this paper consist of novel chemistry, abrasive reengineering (further advancement of Adcon technology as reported in previous Adcon NanoCeria™ paper [3]), localization of various raw materials used in slurry, point-of-use-preparation, and the technology that enables slurry recycling in semiconductor volume production. These Adcon technologies have successfully reduced CMP CoO (improved CMP performance and reduced cost) in the 1st pass at a volume production fab of standard semiconductor products.

Results and Discussion

On-Site Production of Nanometer CMP Slurry

Advanced CMP slurry was produced on-site using highly concentrated colloidal silica A manufactured oversea with the locally-produced and concentrated mixture (including NanoCeria™-like components) by locally-trained engineering staffs. The entire process is standardized and following ISO9002 guidelines by a team of technical staffs trained in advance. In simulated runs ahead of time, the consistency of the slurry in different stages of slurry production and CMP operation were thoroughly tested, in terms of the nanometer particle size distribution, abrasive particle composition, solution chemistry (including additive concentration, pH, conductivity, and trace metal ion concentration), rheological and tribological properties (including viscosity and other temperature sensitive properties), and surface and interfacial properties of abrasive particulates and the materials being polished away during the processes (including zeta-potentials as shown in Figure 1 for one of reference and intermediate slurry samples for QC and QA). Selected parameters were sampled during production in the fab to verify the consistent quality of the slurry and the robustness of the process implemented on the production line. In addition, as a process control measure, the temperature of pad and the slurry in the recycling tank was monitored throughout the production run to ensure the repeatability of each batch until the end of the recycling life.

Newly designed slurries containing 20nm and 60nm silica particles (as shown in Figures 2 and 3) and minute amount of Adcon NanoCeria™ (as an option for improved CMP performance [3]) proved during a >3000-wafer continued run in volume production of standard Si wafer products that >50% CoO/CoC reduction was achieved by using the 1st-ever locally manufactured CMP slurry at semiconductor-manufacturing site in China and recycling the slurry during Si wafer production, thus minimizing high shipping cost for moving large volume diluted slurries (containing components originally manufactured in China) across the ocean and reducing slurry consumption by orders of magnitudes for each yielding Si wafer in production. Furthermore, higher Environmental, Health and Safety standard was enforced by slurry recycling and reduction of water usage and chemicals usage at a leading semiconductor manufacturing fab in China.

Defect Reduction by New Nanometer Slurry

As shown in Figure 4, the new slurry significantly improved defect performance as compared to the spec. The 1st pass yield (passing particle spec) by using the new slurry was as high as 98% for a 400-wafer continued run when 100% wafers were sampled for complete measurements. Among all the wafers, 92% wafers showed no scratches and 96% showed no stains. Through the 100% wafer inspection, the similar trend in defect reduction was also observed in the 3000-wafer extended production run and the larger wafer polishing as a sanity check. The improved performance is attributed to the higher quality and controllability of the new slurry, in terms of the particle size distribution, solution chemistry, rheological and tribological properties, and surface and interfacial properties of abrasive particulates.

Planarity Improvement by New Nanometer Slurry

As shown in Figures 5 and 6, the new slurry significantly improved both global flatness and local flatness as compared to the spec. Through the 100% wafer inspection, the similar results in planarity improvement were also obtained in the 3000-wafer extended production run and the larger wafer polishing for higher technology nodes. The improved CMP planarity performance is mainly attributed to the higher quality and controllability of the new slurry, in terms of solution chemistry, tribological properties, and interfacial properties of abrasive particulates.

Conclusions

New slurries containing 20nm and 60nm silica particles and minute amount of Adcon NanoCeria™ (as an option for improved CMP performance) proved during a >3000-wafer continued run in volume production of standard Si wafer products that >50% CoO/CoC reduction and improved planarity and reduced defects were achieved by using the 1st-ever locally manufactured CMP slurry at semiconductor-manufacturing site in China and recycling the slurry during Si wafer production.

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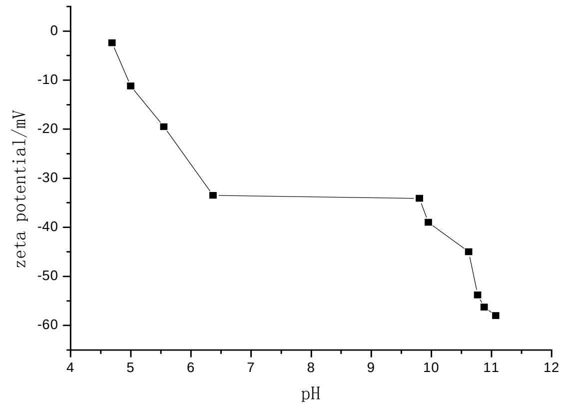

Figure 1. Zeta-potential vs. pH for one of reference and intermediate slurry samples tested for QC and QA

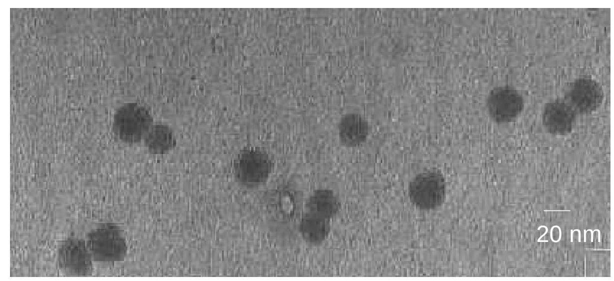

Figure 2. TEM micrograph of 20nm colloidal silica

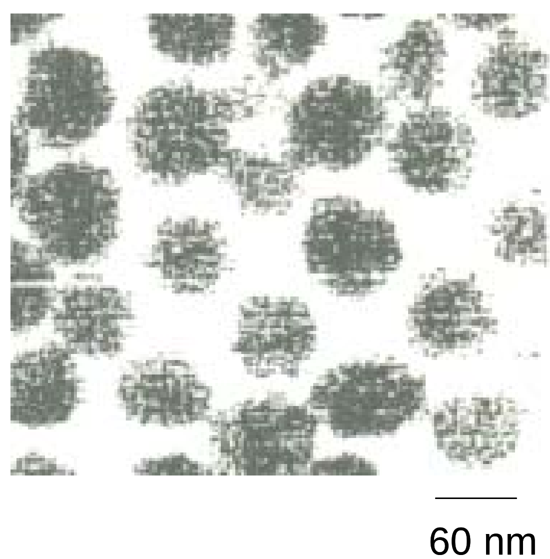

Figure 3. TEM micrograph of 60nm silica particulates

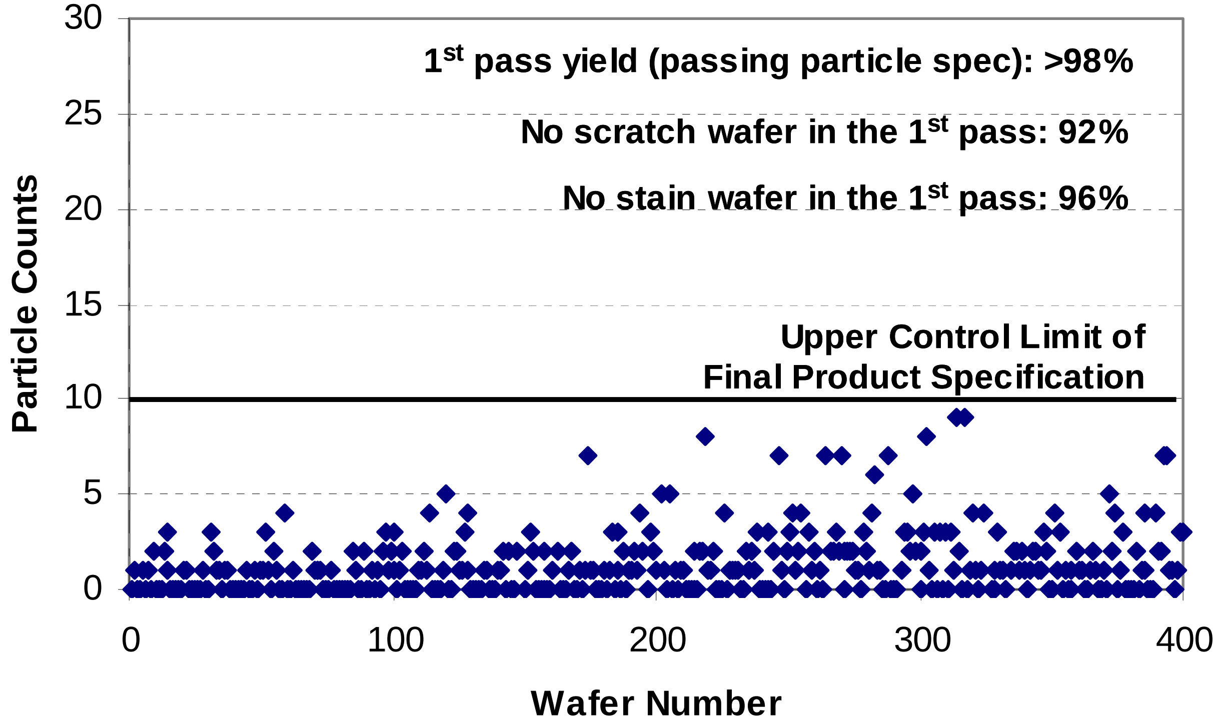

Figure 4. Particle counts measured in the 100% wafer inspections during a continued volume production run

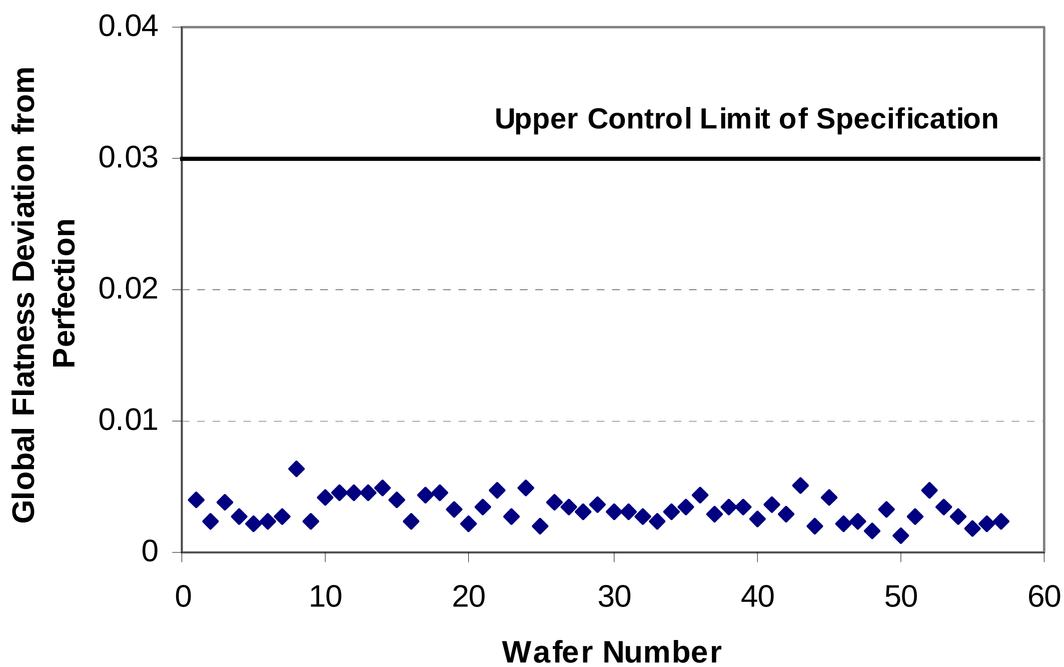

Figure 5. Global planarity measured in the 100% wafer inspections during a continued volume production run

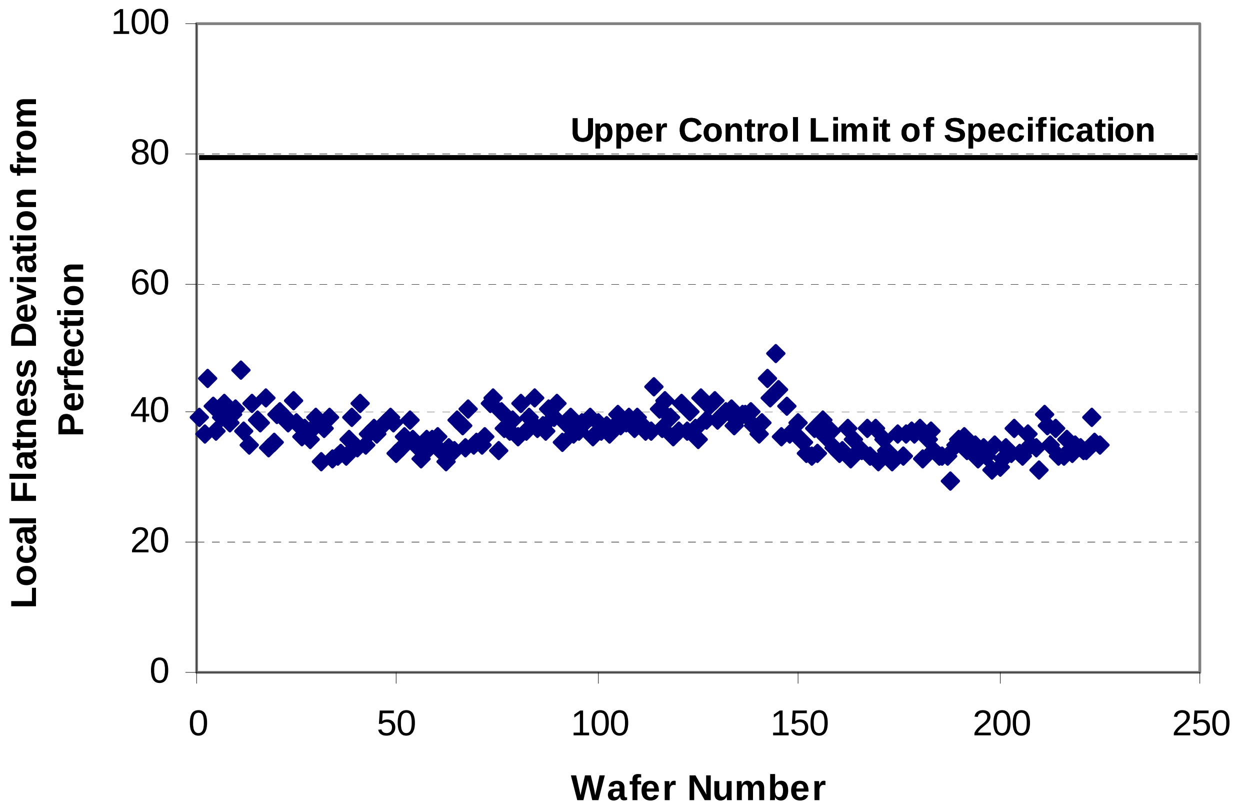

Figure 6. Local planarity measured in the 100% wafer inspections during a continued volume production run

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