IMPACT OF CMP/CLEANING CONSUMABLES ON IC DEVICE YIELD AND PROCESS MODULE COO

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This paper reports technology advancements of NanoCeria® CMP slurries (utilizing nanometer ceria abrasive particulates of pseudo-spherical shape and controlled size distribution) and CY18™ cleaning solutions (designed for removing yield-killer defects and enabling IC device integrity) at semiconductor fabs. Both the CMP slurries and the wet cleaning solutions increased IC device yield by more than 30% and significantly reduced CMP/cleaning process module CoO at different semiconductor fabs. In addition, low cost by design in a global supply food-chain and partnership with IC fab customers are important for a CMP/cleaning consumable manufacturer to be a long-term global industry leader and to achieve the sustainability of long term business growth.

INTRODUCTION

In a typical IC fab, yield killer defects generated by CMP/cleaning frequently ranked the top three in the defect Pareto charts on the fab operation radar screen, almost as serious as lithography generated defects [1]. To effectively and efficiently reduce these yield killer defects, more fab/supplier (materials and equipment manufacturers) partnership has to be fostered. In early stage of semiconductor industry, all IC manufacturing materials and wafer fab equipments (WFE) were developed by a few leading IC fabs, out of the necessity and practicality. Over the decades of industry development and CMOS and BiCMOS technology maturing, more and more IC fab materials and equipments along with processes/recipes are standardized and supplied globally by major fab materials and equipment manufacturers. However, a reverse trend is being noticed, at least in critical materials and processes, for the advanced technology nodes in the ever-faster IC device critical dimension shrinking, the onset of billion transistors packed in a single IC chip today, and nano-electronics on the horizon. More and more early stage materials and processes R&D or screenings are being conducted directly in IC fabs, due to application specific and IC device sensitive nature of critical fab materials and processes, such as some of CMP/cleaning consumable materials, especially for the critical process modules including direct STI (Shallow Trench Isolation) CMP at 130nm technology node and beyond. In this new trend or slow-down of the old trend, some leading fabs are already actively searching for their right partners among fab materials and equipment companies who are leaders by their technologies, their relevant talent pools, lower-cost-by-design, and fab-friendly business models [2].

These top contenders for productive fab/supplier partnership may not be big or conventional chemicals and materials companies and sometimes more parties are involved to bring in every party's strength in the overall supply food-chain.

In this paper, case studies of fab/supplier partnership in both CMP and cleaning applications are reported to illustrate the following key points in potentially fostering more productive fab/supplier partnership aiming for improved IC device yield and reduced manufacturing CoO:

- Key technology is more important than large pool of resources residing outside of fab, even the technology currently resides only at a small supplier/company
- Low cost by design in a global supply food-chain is more important than a large supplier alone who can sustain operation loss for a long time
- Mutual trust (by sharing vital information) for long-term win-win is more important than a short-term return on investment (ROI) that helps only quarterly financial results at its own organization.

In Case Study #1, Fab G reduced CoO by more than 50% at significantly improved yield. In Case Study #2, Fab C improved IC device yield by more than 30% across IC product lines during progressive technology product manufacturing ramp while continuing CoO reduction. In this paper, mechanism of the technologies (mainly related to size and shape tunable nanometer ceria based slurries (Adcon NanoCeria®) [3-5] and Adcon CY18™ cleaning solutions employeed in the case studies will also be discussed to explain the significant yield/CoO improvement achieved on volume production lines.

IMPACT OF ADVANCED CMP SLURRIES ON YIELD AND COO

Recent technology advancement has proved in leading IC fabs that yield killer defects generated during the critical CMP (e.g., direct STI CMP) step were directly responsible for more than 50% of entire CoO for the specific CMP process step, as shown in Figure 1. In other words, at a given critical CMP step (e.g., direct STI CMP), the IC device yield loss due solely to CMP defects out-weighed all other manufacturing costs, ranging from CMP/cleaning consumables costs, CMP/cleaning equipment depreciation costs, skilled labor costs, and yield management costs. For the direct STI CMP step at a leading IC fab, nearly 90% of IC device yield loss was attributed to the current leakages or shorts generated by large and/or irregular-shaped rigid abrasive particulates induced defects during the CMP process, as shown in Figure 2.

In the first case study, the results shown that NanoCeria® and NanoSilica™ CMP slurries (developed and manufactured by Adcon Lab Inc.) significantly improved the production fab yield and CoO.

Large and/or irregular shaped particles (especially micrometer ceria abrasive particles as contained in commercial ceria CMP slurries currently sold on the market) have been confirmed to be the root cause of majority yield-killer defects encountered at a critical CMP step (direct STI step using ceria slurry) in semiconductor fabs. As a temperary remedy to the slurry problems, IC fab engineers have to introduce extra slurry processing

steps and apply extra measures to minimize the damages induced by these CMP slurries containing micrometer ceria abrasive particles and alike. As shown in Figure 3, these less desirable abrasive particles have either large particle sizes and irregular particle shapes (for ceria) or a tentency to form hard particle aggregates on CMP systems and slurry delivery systems due to their relatively high solid contents and formulation deficiency (for some of silica based products).

During CMP process, large and/or irregular shaped particles (from slurries) will have a tendency to rip off a portion of materials in the dielectric films (being planarized), thus forming chartter marks (wide and deep marks or macroscratches), microscratches, and pits (craters formed due to initially embeded particles on the films being planarized). All these defects (induced by large and/or irregular shaped particles) will offer "shelters" for the conducting materials during following process steps (required for manufacturing IC devices) and lead to the shorts on IC devices at various testing and usage stages: (1) immediate IC circuitry breakdown and thus low initial sort yield, (2) current leakage developed over the time and thus poor reliability.

As shown in Figure 4, large and/or irregular shaped particles contained in a mainstream ceria slurry used in today's IC fab production has tendency to lead to the pits as observed on dielectric film during polysilicon CMP process, another critical CMP step employed by leading IC fabs [3]. However, as shown in Figure 5, the CMP induced yield-killer defects (including the pits as observed) were eliminated by switching to Adcon NanoCeria® based slurries [3]. When applied to STI CMP as shown in Figure 6, Adcon NanoCeria® CMP slurry resulted in more than 40% defect reduction as compared to a current mainstream ceria slurry for STI applications in IC fabs, as shown by SP-1 particle and microscratch counts at 180nm [3]. Defect and yield improvement potential by nanometer ceria slurry as demostrated here has already received a lot of attentions from leading IC fabs [2].

Adcon NanoCeria® and NanoSilica™ CMP slurries have successfully showed significant impact on production fab yield and CoO [5]. The new slurry significantly reduced defects as compared to the process of record (POR). Using the new slurry, the 1st pass yield (passing particle spec) was as high as 98% for a >3000-wafer continued run when 100% wafers were sampled for complete measurements. During 3-day continued volume production run, more than 50% CoO/CoC reduction, improved planarity and reduced defects were achieved using advanced nano-abrasive technologies, locallized raw materials (used in manufacturing CMP slurries) and locally trained engineering staffs at a semiconductor production fab located at a high growth region of semiconductor industry.

IMPACT OF ADCVANCED CLEANING SOLUTIONS ON YIELD AND COO

In this case study, Adcon CY18™ cleaning solution was shown to improve IC device yield by more than 30% across IC product lines (including Flash, FPGA, and SRAM devices) during progressive technology product manufacturing ramp while continuing CoO reduction, as compared to the POR on the IC production lines. The Adcon CY18™ cleaning solutions were designed by Adcon scientists after extensive IC wafer-level

cleaning R&D in selecting novel and superior inhibitors and cleaning agents along with advanced modeling investigations based on density function theory.

During cleaning process in advanced IC fabs, it is always challenging to remove all particles and residues after each process module step (including CMP and plasma etch) and/or before each deposition step (including dielectric/metal film deposition or metallization) while leaving other parts of IC device structures/materials (metal or other conductive and/or dielectric films) intact. For example, it is common to see that a commercial cleaning solution effectively removes all particles and residues and at the same time creates significant corrosion on metal interconnects (contacts or vias or metal leads) or results in unacceptable isotropic wet etching on remained dielectric films. Another challenge for desirable cleaning is to remove organic film (or adsorpted surfactants/inhitors) remained on the metal interconnect surfaces after wet cleaning. Because all particles and residues (including organic film remained on metal surfaces) and metal corrosion and unacceptable wet etching (for dielectric films) lead to higher via/contact/sheet resistance or unaccetable current leakage, these defects (i.e., particles, residues, remaining organic films, metal corrosion, and excess wet etching) will result in IC device yield loss. Any improvement in effectively removing these yield-killer defects will significantly help IC fab financial bottomline.

Through extensive IC wafer level reliability investigations, a Pareto chart for yield killer defects was constructed for the different IC devices in real life fabs to establish the priority of minimizing cleaning-related defects. Through screening several commercially available cleaning solutions, Adcon CY18™ cleaning solution stands out as the best candidate to eliminate the identified yield killer defects. As shown in Figure 7, CY18™ cleaning solution improved IC device yield by more than 30% across IC product lines during progressive IC technology product manufacturing ramp while continuing CoO reduction.

As discussed in our previous publication [5] for CMP slurries (such as Adcon NanoCeria® and NanoSilica™), in order to secure a long-term global industry leadership or even just to achieve the sustainability of long term business growth, it is vital for a cleaning solution and/or CMP slurry manufacturer to locallize raw materials (used in CMP slurry or cleaning solution manufacturing), and to train and hire local engineering staffs at the vicinity of major semiconductor production fabs located at high growth regions of semiconductor industry. Cost of engieering labors and raw material operation is a smaller part of this changing requirement to achieve sustainable bsuiness competiveness in this already integrated global semiconductor industry. The greater part of this changing requirement is to be closer to IC fab customers who are representing growing percentage of future CMP/cleaning consumable purchasing power in this industry. Localization of CMP/cleaning consumable R&D, application, and manufacturing is becoming the basic long term business growth requirement (no longer as an alternative or option, as viewed in the past), as IC manufacturing technonology continuously advances in Moore's law era or post Moore's law era, along with growing supports of foundry business and oursource model (one fab for manufacturing a variety of IC devices from several fabless design houses or IDM companies).

SUMMARY

Both CMP slurries and wet cleaning solutions have significant impact on IC device yield and CMP/cleaning process module CoO. Adcon nanotechnology based CMP slurries (including NanoCeria® slurries) and Adcon CY18™ cleaning solutions have showed their effectiveness in significantly increasing device yield (by more than 30% for CY18™ cleaning) and reducing CMP/cleaning module CoO in different semiconductor fabs. In addition, low cost by design in a global supply food-chain is important to be a long-term global industry leader and to achieve the sustainability of long term business growth. To achieve low cost by design, a CMP/cleaning consumable manufacturer has to hire and train local engineering staffs, form strong win-win partnership inside fab and localize raw materials and manufacturing at the vicinity of major semiconductor production fabs located at high growth regions of semiconductor industry.

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ACKNOWLEDGMENTS

Vision and hardwork of numerous engineers and managers at leading semiconductor fabs are foundation and building blocks for this work. Among many Adcon contributors to this work are James Li, Zhenghe Xu, Guowei He, Jianjun Liu, Fuliang Wu, Ping Jian, Jason Li, Juli Jin, Xuanling Sheng, Jianfeng Wang, Jian S. Hu, John Lyons, Xiaolan Song, and Julius Chou.

BIOGRAPHY

Raymond Jin was a Ph.D. graduate with honor from University of Utah in 1988. He has 16 years of industrial experience as a hands-on technologist and manager in oxide-CMP/STI-CMP/polysilicon-CMP/Si-CMP/low-k-dielectric-CMP/W-CMP/Cu-CMP, material/chemistry R&D, equipment/materials selection, and 0.5μm/0.35μm/0.25μm/0.18μm/0.13μm/90nm/65nm front/back end CMOS/BiCMOS process development/integration/technology transferring. He was credited for a leadership role in improving IC device yield by >30% in both memory and analog/mixed-signal fabs. He worked at leading semiconductor companies, including Applied Materials and National Semiconductor. He also introduced CMP to leading Chinese scientists that later lead to the 1st CMP Ph.D. graduated in China. He is currently CEO/CTO of Adcon Lab, Inc., a global provider of CMP and cleaning solutions and a technology developer and manufacturer of CY18™, NanoCeria®, NanoAlumina™, NanoSilica™, NanoOxidant™, NanoInhibit™, and other products (including the broadest test wafers and IC fab services on the market, teamed up with leading IC fabs) for CMP/cleaning applications. He has 35 technical publications and several patents issued and filed.

Jerry Diao graduated from University of California at Berkley with a Ph.D. in Materials Science and Applied Surface Chemistry in 1990. He has 20 years of industry and academic experience in colloidal and surface chemistry, including slurry, polishing, cleaning, and metrology for semiconductor manufacturing. He joined Adcon in 1994 and is currently a principal engineer and technology program director at Adcon, in developing nano-technology abrasives and CMP slurries as well as cleaning solutions for semiconductor manufacturing. He was a technology leader in designing and developing Adcon CY18™ cleaner, successfully commercialized in different IC fabs and enabled significant yield improvement in volume production of SRAM, Flash, and FPGA IC chips. He has 15 technical publications in the fields of applied surface and colloid chemistry, characterization of surface properties of materials and fine particles, dispersion and stability of fine particles in aqueous suspensions, and rheology of concentrated slurries.

Franklin Xu was a graduate with distinction from New York Institute of Technology, a M.S. in Computer Science along with extensive EE training in 1999. He has 20 years of semiconductor and electronic product development experience, specializing in Embedded System, SoC (System On Chip) design, and ASIC and other IC chip testing. He worked for different semiconductor companies, including Samsung. He is currently a staff engineer and product manager at Adcon and has been involved in test wafer design, manufacturing, and IC fab services aimed for yield improvement and CoO reduction for last three years. In his earlier career, he worked at National Engineering Research Center in China and won the First Prize of Science & Technology Advance, granted by central government.

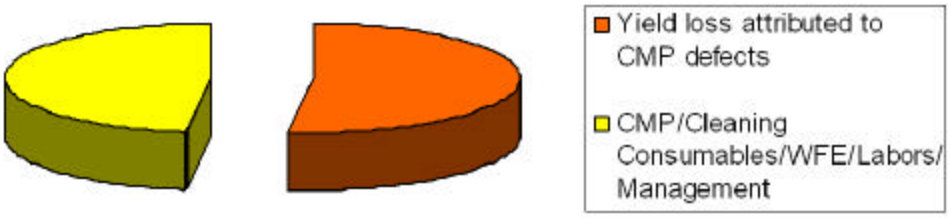

Figure 1. Benchmark of CoO performance at direct STI CMP in volume production fabs.

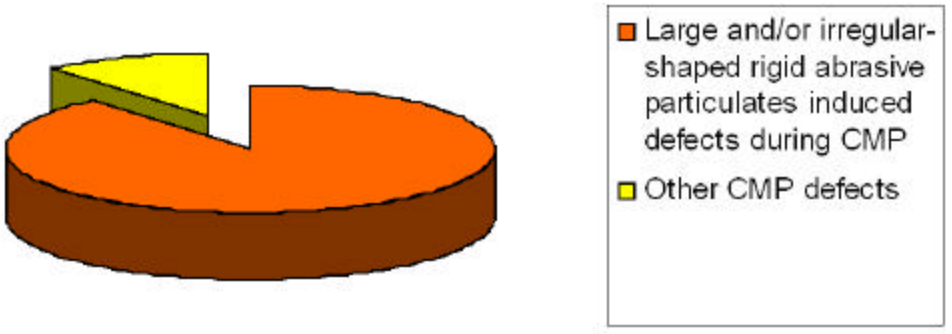

Figure 2. Benchmark of IC device yield loss due to the defects generated during direct STI CMP in volume production fabs.

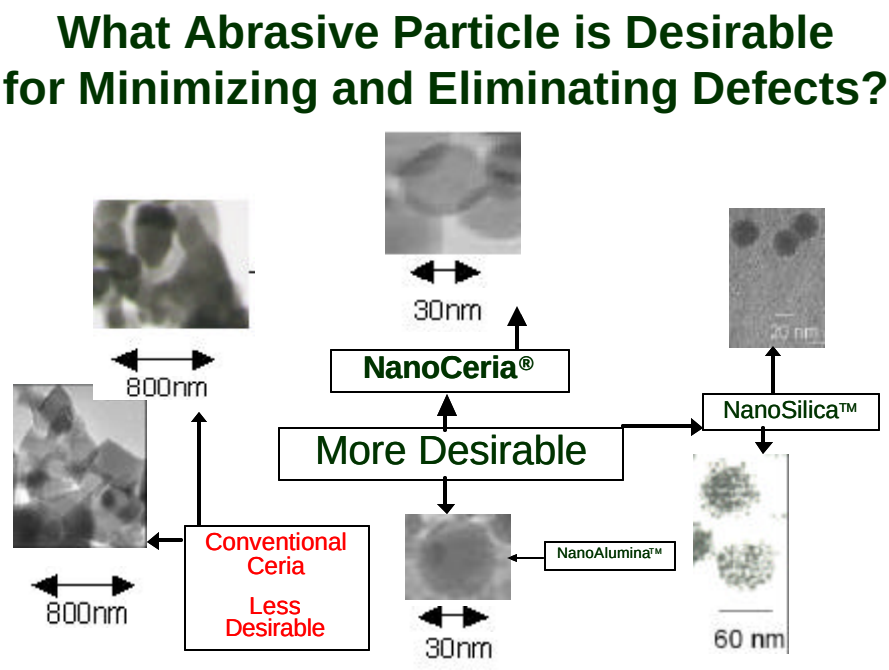

Figure 3. TEM micrographs showing the sizes and shapes of abrasive particles in CMP slurries designed for eliminating CMP defects during IC manufacturing, as compared to a POR/benchmark slurry used in IC fabs

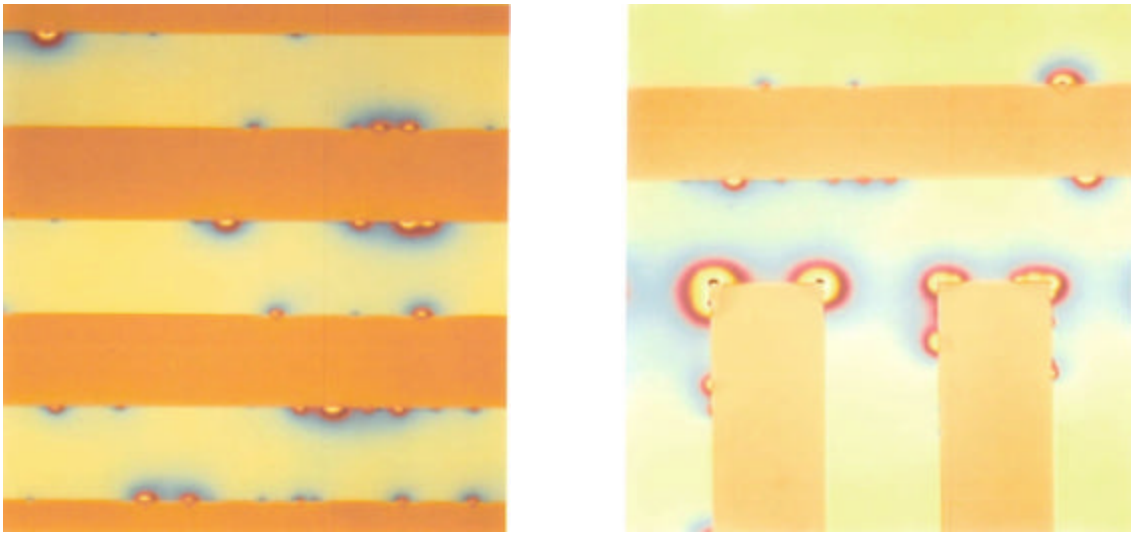

Figure 4. Optical micrographs showing the pitting problems created by large and/or irregular shaped abrasive particles with a POR/benchmark ceria slurry used in the IC fabs.

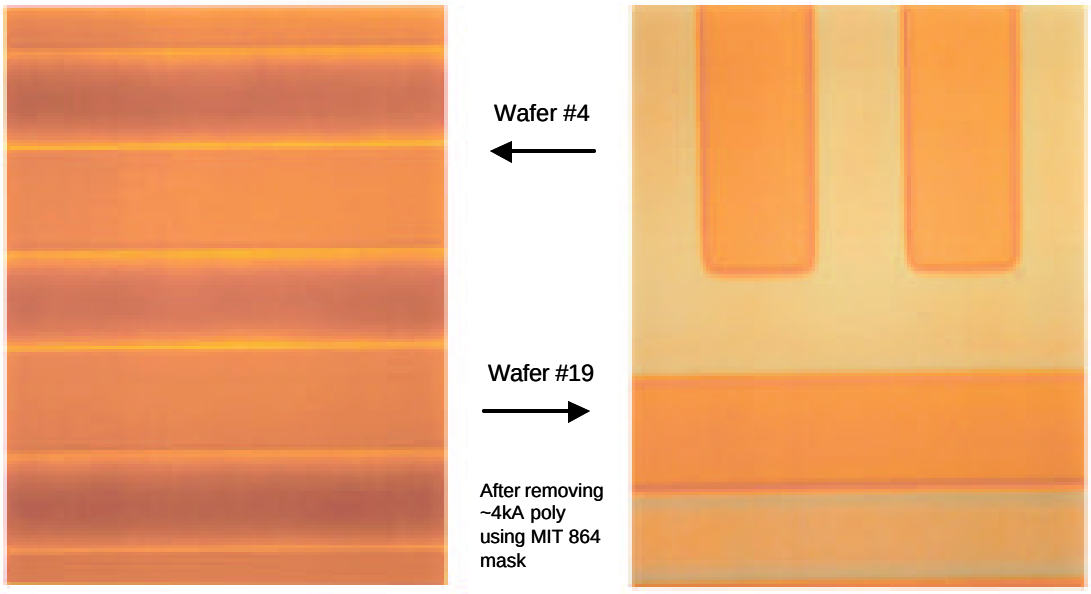

Figure 5. Optical micrographs showing the pitting-free surfaces after completing planarization using an Adcon NanoCeria® based slurry. Notes: The identical photo mask (MIT864, for the patterned polysilicon wafers) and the same CMP/ metrology systems were used for collecting the results shown in both Figures. 4 and 5.

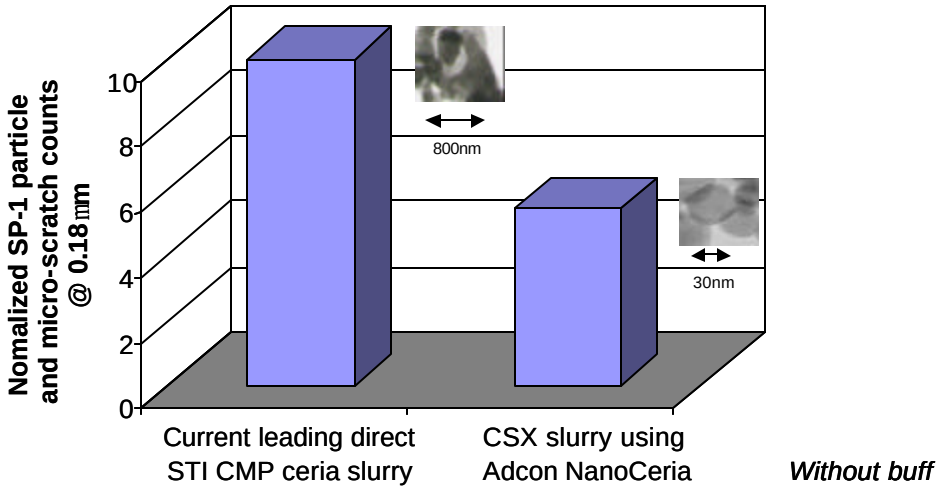

Figure 6. Impact of Adcon NanoCeria® CMP slurry on the particle and micro-scratch counts at the PECVD Teos film of 200mm wafers, as compared to a POR/mainstream ceria slurry for STI applications in IC fabs.

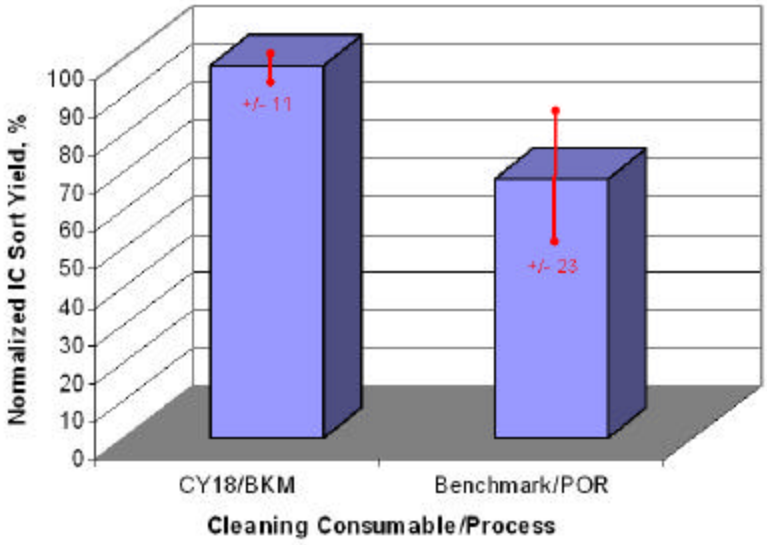

Figure 7. Impact of Adcon CY18™ cleaning solution on the IC device yield.

This paper is for an invited oral presentation at ECS/SEMI International Semiconductor Technology Conference (ISTC), March 15 - 17, 2005, Shanghai, China. This paper is featured in Semiconductor Technology (ISTC2005), Ming Yang, editor, Proceedings of the 4th International Conference on Semiconductor Technology, Volume 2005-08, pp. 657-665, sponsored by ECS, IEEE, Japan Society of Applied Physics, and Sematech International, published by The Electrochemical Society, Inc., 2005.