Nanometer ceria slurries for front-end CMP applications, extendable to 65nm technology node and beyond

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Abstract:

This paper reviews and reports recent technology advancements in front-end CMP (especially polysilicon CMP) applications using nanometer ceria based slurries and other commercially available slurries. [1-3]

In advancing IC manufacturing technologies into 65nm and beyond, front-end CMP (STI, polysilicon, and PMD) has become the most difficult process technology to develop and optimize in order to achieve desirable IC device sort yield. Over the years, polysilicon CMP has been a critical part of process module in the polysilicon plug and polysilicon capacitor formation for both trench capacitor and crown capacitor at almost all advanced DRAM manufacturing fabs. For years at a leading advanced logic IC manufacturer, polysilicon CMP as a process of the record (POR) was also a solution for front-end integration problems arising from the polysilicon gate formation steps in high volume IC device production. On the horizon, the polysilicon CMP along with dielectric CMP has been an enabling technology in metal gate formation to solve the challenging problems of polysilicon depletion at gate oxide interface and thus rising gate sheet resistance. Either polysilicon damascene (stopping on the dielectric layer) or polysilicon planarization (stopping in polysilicon) has been main stream process technology in many new IC device manufacturing in embedded DRAM, advanced flash, various logic (microprocessor and ASIC) applications.

In all front-end applications, CMP engineers are facing technical challenges in both volume production fabs and R&D to continuously minimize the particle-induced defects and micro-scratches and improve the planarity with or without polishing-stop layers. The micro-scratches, particles, excess-erosion of polishing-stop layer, and larger step height or step height variation as compared to more and more tight design rules in advanced technology nodes are key contributors to device yield loss, due to stringers/bridging, current leakage, out-of-spec shift of many electrical parameters, including delta W (difference between electrical and drawn island width) and drive currents of narrow width devices, diode leakage for borderless contacts, Nwell sheet resistance (if the Nwell resistor is under the field oxide and the Nwell implant is after the STI CMP). As a band-aid due to poor CMP performance with conventional slurries on the market today, many expensive process steps are reluctantly added into the current process flow before front-end CMP steps in advanced IC manufacturing, resulting in added manufacturing cost, as high as $25/wafer for STI alone.

Recent efforts at DuPont Electronic Technologies and other R&D fabs in developing and commercializing slurries based on the 1st commercially available round-shaped 30nm colloidal ceria suspensions (Fig. 1) developed and being patented by Adcon Lab have revealed significantly improved performance of the new slurries in terms of planarity and defect reduction potential in front-end CMP (especially polysilicon CMP) applications. When Adcon-designed polysilicon patterned test wafers with MIT 864 mask were used to mimic the IC device structures, the remaining step height at both 100um feature and 50% density areas are improved by more than 3 times as compared to conventional silica based slurries used in volume IC production fabs as shown in Table 1. A formulation of high planarity and high removal rate slurry produced < 50A remaining step height at 100um feature area and <80A remaining step height at 50% density area. Different types of films (including doped or un-doped crystalline polysilicon and amorphous silicon) were used to confirm improved CMP performance by new slurries. When compared to polycrystalline ceria slurries available on the market, the new slurries using round-shaped 30nm colloidal ceria also significantly improved the defects of both patterned and blanket wafers, as manifested by eliminated pits and micro-scratches. The similar CMP performance improvements were observed in preliminary front-end CMP experiments for both STI and PMD applications. For all front-end CMP applications, the new slurries have potentials to provide higher planarity and lower defects at an equivalent polish removal rate to conventional silica or polycrystalline ceria-based slurries available on the market today.

References:

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Biography:
Cass Shang is a R&D chemist at DuPont EKC Technologies with more than 11 years of industrial experience. Her focus at the CMP group is developing new CMP slurries and CMP processes. She has also worked on post CMP cleaning chemistries and processes. Cass has a BS in chemical engineering from Beijing University and an MS in environmental and surface analysis from University of Colorado. She has coauthored 12 papers related to CMP and post CMP cleaning and several patent applications.

Robert Small is the technical director of the CMP group at DuPont EKC Technologies. He is involved in developing new chemistries for post CMP cleaning, CMP chemistries and post etch residue removal. Bob has BS from Norwich University, an MS from Texas Tech University, and a Ph.D. in organic photochemistry from the University of Arizona. He has authored or co-authored over 100 articles and presentations including BEOL, post clean treatment, post CMP and CMP processes. He holds more than twenty U.S. and foreign patents and has ten submitted U.S. patent applications.

Raymond Jin was a graduate with honor from University of Utah, a Ph.D. in Metallurgy and Materials Science in 1988. He has 15 years of industrial experience as a senior technologist, program manager, technology group head, global product/marketing manager in oxide-CMP/STI-CMP/ polysilicon-CMP/Si-CMP/low-k dielectric-CMP/W-CMP/Cu-CMP, new material/chemistry R&D, capital equipment selection, and 0.5um/0.35um/0.25um/0.18um/0.13um front/back end CMOS/BiCMOS process module development/integration/technology transferring. He was credited for a leadership role in improving die yield by 30% in a memory fab and by 40% in an analog/mixed-signal fab. In his industry career, he worked at Applied Materials, National Semiconductor, Cypress Semiconductor and Pilkington. He is currently President and Chief Technical Official of Adcon Lab, Inc., a global provider of CMP and cleaning solutions including the broadest test wafer selections, a technology developer and manufacturer of the 1st commercially available nanometer size colloidal ceria suspensions for CMP applications. He has 32 technical publications, more than 20 presentations at international technical conferences and several patents issued and filed.

Figure 1. TEM micrograph of nanometer abrasives used in Adcon NanoCeria™-30 products.

Table 1. Planarity improvement by nanometer ceria slurries based on Adcon NanoCeria™ series for planarity (without polishing stop layer) applications.

Results were achieved when polishing was stopped in polysilicon, i.e., without a polishing stop layer.	Remaining Step Height at 50% density area, Å (*improvement over baseline*)	Remaining Step Height at 100um features, Å (*improvement over baseline*)
Current baseline (silica based), In literature & volume production	>600	>800
High removal rate, CSX-01	<200 (*3x*)	<250 (*3x)*
High planarity & low rate, CSX-02	<150 (*4x*)	<100 (*8x*)
High planarity & low rate, CSX-03	<50 (*11x*)	<100 (*8x*)
High planarity & high rate, CSX-08	<80 *(7x)*	<50 *(16x)*

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