Nanometer Ceria Slurries for Front-End CMP Applications, Extendable to 65nm Technology Node and Beyond

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Adcon NanoCeria™ Series

A family of nanometer colloidal ceria suspension products

- Nanometer ceria abrasives in their stable concentrated suspensions with different controlled shapes (including round shapes), customer-specified solid content, customer-desired pH and chemistry, customer-specified size or size distribution, ranging from 10nm to 120nm

- Commercially available with new manufacturing plant design capacity of 20,000 lbs solid equivalent a year and already supplied to three multi-billion $ global companies

- Technology and product R&D, engineering, manufacturing, QC/QA, marketing, sales, and customer support are managed by experienced and western trained semiconductor industry professionals and supported by well-established technology organizations and Chinese government, who makes regulatory policies over the majority of rare earth raw materials on today’s world market

To eliminate defects and micro-scratches and improve planarity in different CMP applications for 65nm technology and beyond
Adcon NanoCeria™-30 TEM, Average 30nm

Designed to eliminate defects and micro-scratches and improve planarity in direct STI CMP application
Defect Reduction and Planarity Improvement by Controlling Ceria-Wafer Interaction Forces

- Forces based on DLVO theory and beyond:
  - Electrical interaction and intra-action between nanometer ceria particles of controllable shape and size distribution and the dielectric films being removed
  - Chemical or other specific interaction and intra-action between nanometer ceria particles and the dielectric films being removed, as induced or impacted by additives
  - Any interaction and intra-action forces (including van der Waal’s, steric hindrance) under specific rheological and tribological conditions with specific pad, conditioning disk, and CMP platform/process

Adcon NanoCeria™ Products used for optimizing CMP performance at 65nm technology
Polysilicon CMP Applications
Poly CMP – Damascene Applications

Oxide film formation (1)
Pattern and etch to form plug or trench (2)
Deposit polysilicon (3)
Remove Polysilicon (4)

- RIE?
- RIE + Oxide CMP
- CMP + RIE
- Poly CMP

Which process provides a better control of recess and stop layer erosion?
**Poly CMP – Planarity Applications**

Adcon NanoCeria™ slurry as a solution for challenging technical problems for CMP engineers in advanced IC fabs.
Poly CMP for Crown Capacitors

A enabling technology for Advanced DRAM
Schematic Diagram of Self Aligned Metal Gate

a Process Flow

Step 1: Oxide deposition

Step 2: Poly CMP after oxide CMP

Step 3: Poly etch

Step 4: Metal deposition

Step 5: Metal CMP

R. Jin et al., 1998. Semicon Taiwan, SEMI IC Seminar Proceedings
Dual Poly Damascene for Poly Gate and Self Aligned Poly Contact

Step 1: STI formation

Step 2: 1st poly damascene -- poly dep.

Step 3: 1st poly damascene -- poly CMP

Step 4: 2nd poly damascene -- poly dep.

Step 5: 2nd poly damascene -- poly CMP

R. Jin et al., 2000. CMP MIC Proceedings
**Improved Planarity by Nanometer Ceria Slurries**

CSX series based on Adcon NanoCeria™ series for both planarity (without polishing stop layer) and damascene (with polishing stop layer) applications

Results were achieved when polishing was stopped in polysilicon, i.e., without a polishing stop layer.

<table>
<thead>
<tr>
<th></th>
<th>Remaining Step Height at 50% density area, Å (improvement over baseline)</th>
<th>Remaining Step Height at 100µm features, Å (improvement over baseline)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current baseline (silica based), In literature &amp; volume production</td>
<td>&gt;600</td>
<td>&gt;800</td>
</tr>
<tr>
<td>High removal rate, CSX-01</td>
<td>&lt;200 (3x)</td>
<td>&lt;250 (3x)</td>
</tr>
<tr>
<td>High planarity &amp; low rate, CSX-02</td>
<td>&lt;150 (4x)</td>
<td>&lt;100 (8x)</td>
</tr>
<tr>
<td>High planarity &amp; low rate, CSX-03</td>
<td>&lt;50 (11x)</td>
<td>&lt;100 (8x)</td>
</tr>
<tr>
<td>High planarity &amp; high rate, CSX-08</td>
<td>&lt;80 (7x)</td>
<td>&lt;50 (16x)</td>
</tr>
</tbody>
</table>

CSX-Series Slurries provide >3x planarity improvement
Pitting Problems with a Current Leading Ceria Slurry in the IC Fab

Current ceria slurry formulation using micro-ceria causes poly pitting
CSX Slurries Based on Adcon NanoCeria™
Products to Solve Pitting Problems

New formulation and Adcon NanoCeria™ engineering prevent pitting

After removing ~4kA poly using MIT 864 mask
Direct STI CMP Applications
Why Direct STI CMP & Adcon NanoCeria™?

Conventional STI CMP (currently >90% fabs):

- Ceria based CMP is the best direct STI solution
- Current micro-ceria causes µ-scratches and creates scares in IC fab
- Adcon NanoCeria™ eliminates µ-scratches and extends IC technologies

~$25/wafer savings by eliminating Reverse Mask steps (tools)
Reduction of Direct STI CMP Defects and μ-Scratches by Adcon NanoCeria™ Slurry

CSX slurry reduces direct STI CMP defects and μ-Scratches @0.18 μm by >40%
Summary

- CSX slurries using Adcon NanoCeria™ products improved polysilicon CMP planarity performance by >3x

- CSX slurries solve front-end CMP defect problems, including pitting, particles and micro-scratches in polysilicon and direct STI CMP applications

- Significantly improved defect performance and planarity (<100A remaining step height without polish stop layer) makes CSX slurry extendable to 65nm technology