A Novel Retaining Ring in Advanced Polishing Head Design for Significantly Improved CMP Performance

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ABSTRACT

This paper reports a technological advancement in developing and implementing a novel retaining ring of advanced edge performance (AEP™ ring) for an advanced polishing head design. The AEP ring has been successfully used for significantly improved CMP performance in different CMP applications: oxide (PMD and ILD), shallow trench isolation (STI), polysilicon, metal (W and Cu), silicon-on-insulator (SOI), and silicon CMP. Robust processes have been developed using AEP ring along with many hardware upgrades for each application with extended runs to meet requirements of advanced IC device fabrication.

INTRODUCTION

The challenge in polishing head design is to assure required CMP process performance (low non-uniformity, high removal rate, low defects, good head-to-head matching, and low-pressure/ high-speed capability), short qualification time, and low cost of ownership. Conventional polishing heads coupled with polyurethane-based polishing pads have a limitation in achieving a low non-uniformity due to the pad deformation at the edge of the wafer during polishing, as manifested by a slow or fast edge polishing rate. In this work, an advanced polishing head (Titan Head™) design has been studied by utilizing different retaining rings. The AEP retaining ring has been developed and implemented to shorten polishing head qualification time and to achieve the CMP process performance required for manufacturing advanced IC devices (e.g., sub-0.25μm and/or mixed signal devices).

EXPERIMENTAL

A 4-head and 3-platen CMP tool (Mirra® CMP system) was used with 8” wafers throughout this work. Different retaining ring designs coupled with a Titan Head design were investigated for improved performance. The Titan Head design features a flexible membrane applying a uniform pressure to the backside of the wafer. The advanced polishing head is equipped with a retaining ring to prevent wafer slippage during polishing. A more important function of the retaining ring in a Titan Head design is to modulate the polishing removal rate near the edge of the wafer for a low within wafer non-uniformity (WIWNU) at reduced edge exclusions. This is achieved by independently controlled pressure applied onto the ring. Two different types of retaining ring materials were used in this work. The first type is a polymeric material requiring lapping. The second type used in different ring designs including the AEP design is the layered materials. The retaining ring made of the first type of material is called P ring in this paper. The new-generation retaining ring (AEP ring) requires no individual modification for fitting, no lapping and no adjustments.

Stacked IC1000/Suba IV pads (Rodel) were used for polishing and a Politex pad (Rodel) was used when buff is applied. For pad conditioning, an improved diamond disk manufactured by using a proprietary high temperature Ni-Cr brazing process was used in conjunction with an advanced conditioner head assembly design. [1] Cabot's SS-12 slurry was used as an oxide slurry. Consumables used in W and polysilicon CMP were described in previous work. [2, 3].

RESULTS AND DISCUSION

Impact of Retaining Ring Design Types on WIWNU

The retaining ring design has a significant impact on WIWNU due to the ring-pad-wafer-membrane interaction (Fig. 1). In a Titan Head design, an independently-controlled pressure (P_1) is applied onto the retaining ring to absorb pad deformation around the wafer edge during polishing. Meanwhile, a uniform pressure (P_2) is applied by a flexible membrane over the wafer backside to achieve a desirable polishing rate. To optimize WIWNU, the retaining rings of different designs were evaluated. The results are summarized in Table 1. The results indicate that an AEP ring design is critical to ensure low WIWNU. The AEP ring design can more effectively control pad deformation during wafer polishing as compared to the conventional P ring. As a results, better edge performance of an AEP ring was achieved than a P ring as shown in wafer scan (Fig. 2).

Impact of Pressure and Speed on Removal Rate and Non-Uniformity

Designed experiments were conducted to optimize the processes for high removal rate and low non-uniformity. The impact of retaining ring pressure and platen speed on removal rate and WIWNU is shown in a contour map (Fig. 3).

The results indicate that WIWNU can be significantly improved by increasing retaining ring pressure in the range studied which is made possible by Titan Head design. At a high retaining ring pressure, WIWNU can also be improved by increasing platen speed at a constant head/platen speed difference. However, when retaining ring pressure is lowered, the trend is different. WIWNU can be improved by decreasing platen speed. The results also indicate that removal rate is proportional to platen speed and insensitive to retaining ring pressure at a constant membrane pressure. Later studies reveal that the contour map is more complicated when speed and pressure are extended to outside of the range studied in this work. [4]

Removal Rate and WIWNU in Oxide CMP Extended Runs: AEP vs. P Ring

An extended run was conducted using AEP rings for 3 heads and a P ring for the fourth head with thermal oxide wafers. The results are summarized in Table 2 and Figs. 4 - 5. Table 2 shows that AEP rings improved wafer-to-wafer non-uniformity (WTWNU) (1.6%) as compared to the P ring (2.5%) in this extended run (called Run #2 in Table 2). The performance of P ring in this extended run (Run #2 in Table 2) is similar to another extended run using P rings on all four heads (Run #1 in Table 2). For comparison, AEP performance from the third extended run using a higher

pressure process and AEP rings on all four heads is also listed in Table 2 as Run #3. The results indicate that WIWNU and removal rate using the AEP ring without lapping are stable and comparable to those with the lapped P ring using the same process (pressure). To achieve acceptable CMP performance at <5 mm edge exclusion, a P ring is always lapped prior to CMP operation. An AEP ring does not require lapping. An AEP ring design ensures precise and uniform pressure control on a polishing pad around the wafer edge.

The AEP ring has been implemented in IC fabrication. An 800-wafer extended run was conducted over three days, the results confirmed the stability of removal rate and WIWNU achieved by an AEP ring (Fig. 6).

Defect Performance Using AEP Ring

After the lapping operation using a conventional lapping tool, macro-scratches and embedded particles from abrasive lapping materials may appear at the working surface of the P ring. The embedded particles could release during subsequent polishing steps and thus scratch the wafer. The AEP ring does not require lapping and thus eliminates the possibility of scratching by embedded abrasive lapping materials and thus provides reduced micro-scratch and defect counts on the wafer surface. Typical defect performance over multiple days using 2-platen polish with the third platen rinse is shown in Fig. 7. The defect counts (>0.20µm, SS6420) are less than 45 (UCL) with average count of 18. The total defect and micro-scratch counts (>0.25µm, SS6200) are less than 88 (UCL) with average count of 33. Similar defect performance was achieved using 3-platen IC1000 polish with the third platen rinse for improved throughput. The average defect count (>0.20µm, SS6420) is 18 and the average total defect and micro-scratch count (>0.25µm, SS6200) is 39 over a 1200-wafer extended run using a 3-platen IC1000 polish.

Customer Performance: AEP vs. P Ring

The AEP ring performance was monitored in a high volume production fab. A test wafer was measured for removal rate, WIWNU and defect every 25 wafers. Over a one-month run, AEP rings significantly improved WIWNU. As compared to P rings, AEP rings reduced average WIWNU by more than 40% to 3% at 5 mm edge exclusion. AEP rings also eliminated all the out-of-control points. AEP rings on two different Mirra tools also showed improvement in defect counts. The improvement by AEP rings as compared to P rings is attributed to the AEP ring design and elimination of lapping. As required, P rings were lapped off-site by different operators on a relatively low-tech lapping tool after each head re-build. Quality of lapped P rings used in a fab is less consistent than that of AEP rings without lapping.

Removal Rate, WIWNU and Defects in a W CMP Extended Run

The AEP ring has been successfully applied to W CMP. [2] A 1600-wafer W CMP extended run has been conducted using an AEP ring. As seen in the oxide CMP application, a stable removal rate (4046 Å/min.) and low and stable non-uniformity (average WIWNU 2.5%, WTWNU 4.1%) was achieved at 5mm edge exclusion (Fig. 8). Defect counts on PETEOS wafers (>0.25µm, SS6200) in the W CMP extended run were kept below 100 for the process with oxide buff.

Removal Rate WIWNU and Defect in a Polysilicon CMP Extended Run

Polysilicon CMP processes using AEP ring have been successfully applied to production of advanced IC devices for both DRAM polysilicon plug formation and polysilicon gate formation. [3] An AEP ring was used in a polysilicon CMP extended run. The results are presented in Fig. 9. As in the case of oxide and W CMP applications, the AEP ring ensured a low and stable WIWNU (2.7%, Fig. 9) and a stable removal rate (3609 Å/min. on average). The average total defect and micro-scratch count (>0.16μm, SS6200) from 18 polysilicon monitor wafers is 25 using an optimized process.

Other CMP Applications Using AEP Ring

AEP ring coupled with Titan Head design and optimized processes has contributed to wide acceptance of the Mirra CMP platform for oxide (PMD and ILD), STI, polysilicon, as well as W CMP applications in IC fabs.[5] The AEP ring along with many other hardware upgrades has also played an important role in successful Cu, SOI, and Si CMP applications on the Mirra CMP platform. [6]

CONCLUSIONS

The retaining ring used in an advanced polishing head design improves WIWNU by modulating pad deformation and controlling the removal rate around the wafer edge. WIWNU and removal rate depend on pressure and the head/platen rotating speed. Through designed experiments, CMP processes can be optimized to achieve low WIWNU, high removal rate, and stability. As compared to the first generation retaining ring, the retaining ring of novel design (i.e., AEP ring) significantly improves CMP performance. The AEP ring eliminates lapping, thus reduces qualification time, improves WIWNU and WTWNU, and reduces defect and micro-scratch counts. To meet the requirements of advanced IC device fabrication, the AEP ring coupled with Titan Head design along with many hardware upgrades and optimized processes on the Mirra CMP platform are proved to be effective in different CMP applications, including oxide (PMD and ILD), STI, polysilicon, W, Cu, SOI, and Si CMP.

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Table 1. WIWNU as a function of retaining ring design types.

Retaining Ring Design Types	WIWNU at 5mm EE
AEP	1.0 to 3.0%
Alter_A	2.4 to 3.0%
Alter_B	3.1 to 4.0%
Alter_C	8 to 14%

Table 2. Removal rate and WIWNU with AEP ring as compared to P ring in extended runs. (Run #2 presented in Fig. 4. A different process at higher pressure used in Run #3).

Type of Retaining Ring Extended Run #	P Run #1	P Run #2	AEP Run #2	AEP Run #3
Process Performance				
Thermal Oxide Removal Rate (A/min)	2,900	3,000	3,000	4,050
PETEOS Removal Rate (A/min)	3,600	3,750	3,750	5,050
WIWNU (5mmEE-1s)	3.2%	2.7%	2.9%	2.0%
WTWNU (5mmEE-1s)	2.1%	2.5%	1.6%	2.6%

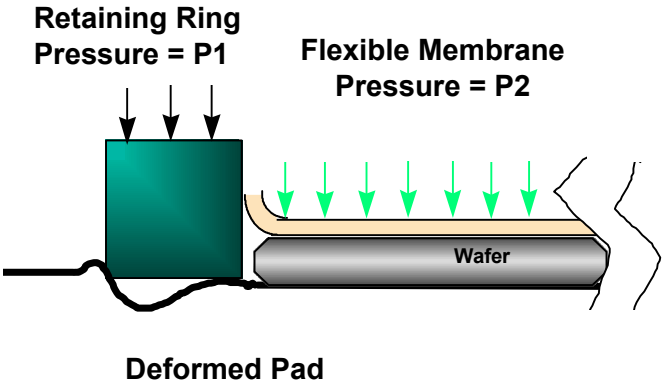

Fig. 1. Schematic diagram of retaining-ring/pad/wafer/membrane interaction.

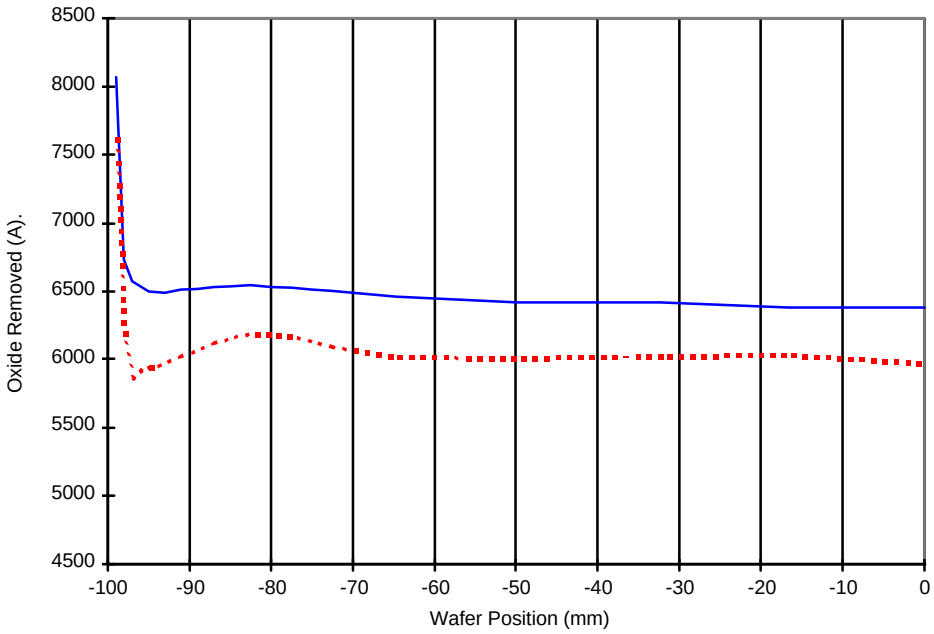

Fig. 2. Wafer scan from AEP (solid line) and P (dotted line) retaining rings using an optimized process.

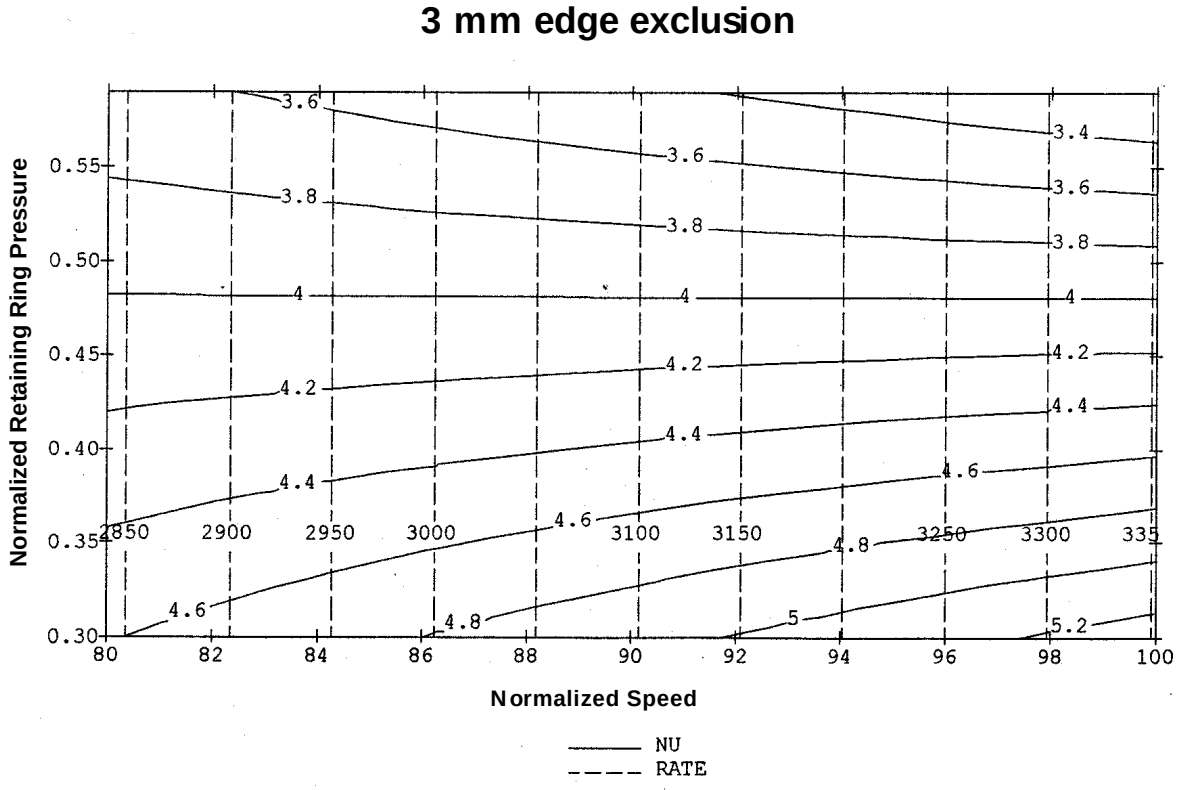

Fig. 3. Oxide removal rate and WIWNU (3 mm EE) contour map plotted against normalized platen speed and normalized retaining ring pressure at a constant membrane pressure and a constant head/platen speed difference.

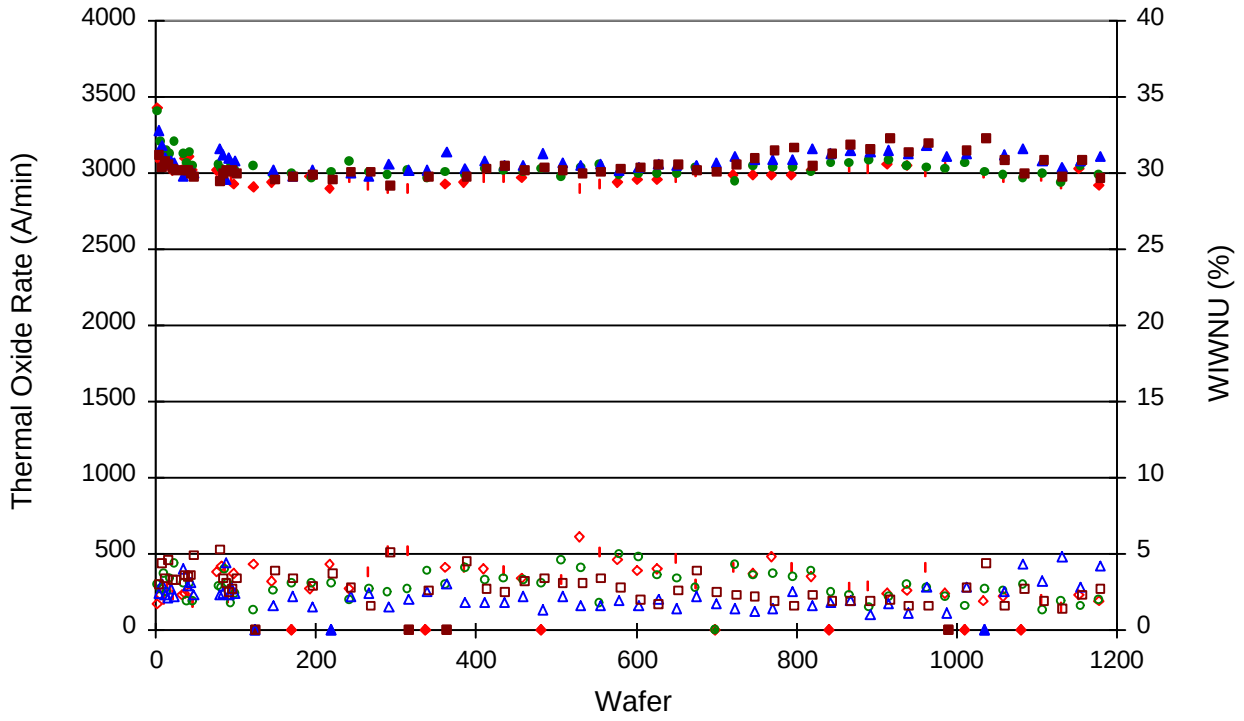

Fig. 4. An extended run using AEP rings for 3 heads and a P ring (square symbol) for the fourth head with thermal oxide wafers at 5 mm edge exclusion.

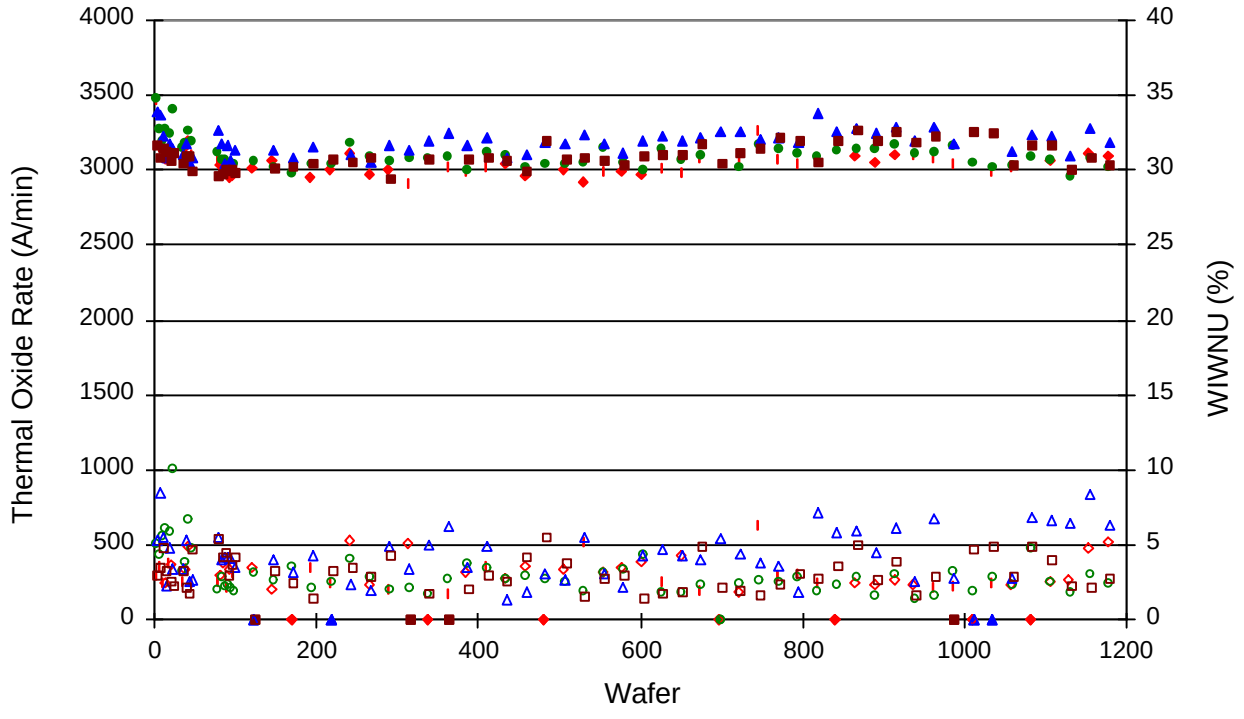

Fig. 5. An extended run using AEP rings for 3 heads and a P ring (square symbol) for the fourth head with thermal oxide wafers at 3 mm edge exclusion.

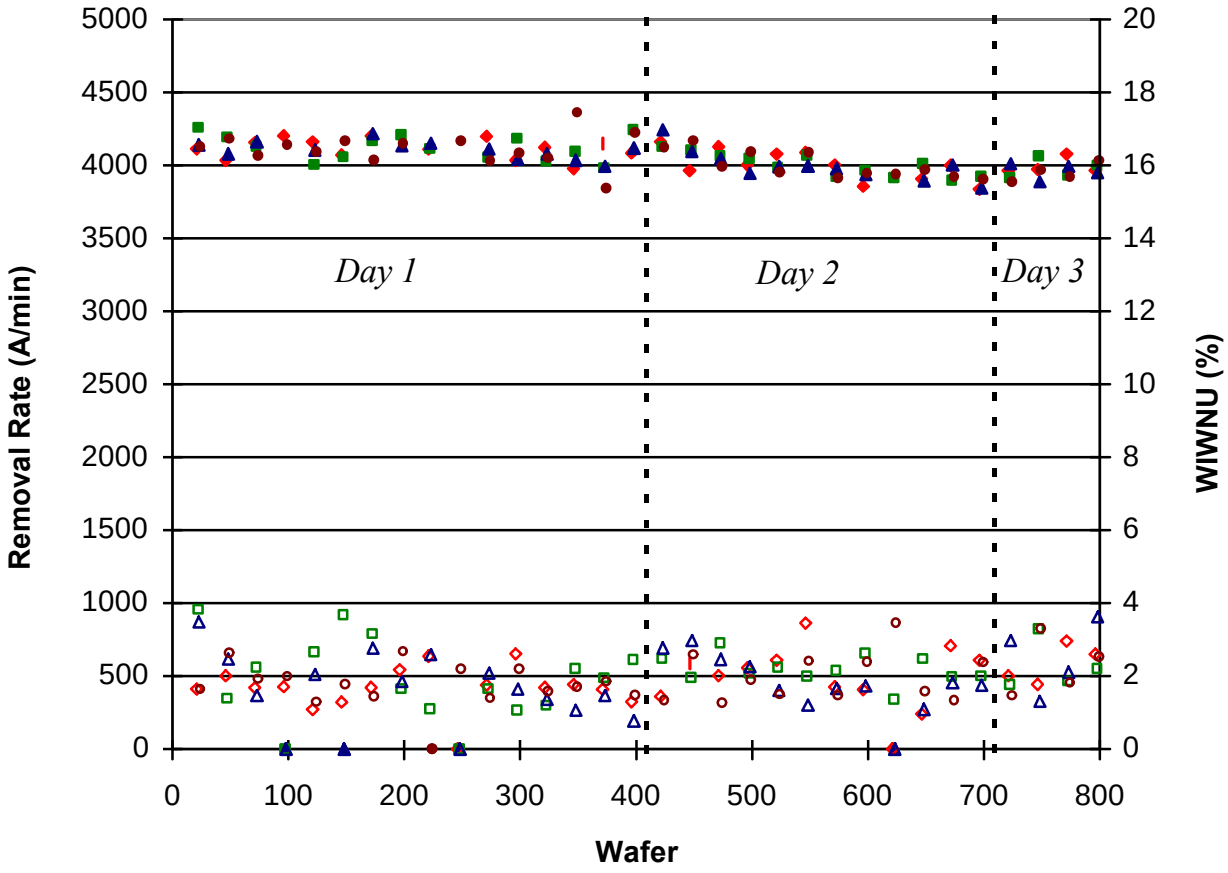

Fig. 6. An extended run over 3 days using AEP ring with oxide wafers at 5 mm edge exclusion. Avg. removal rate = 4053 Å/min. Avg. WIWNU = 2.0%. WTWNU = 2.6%.

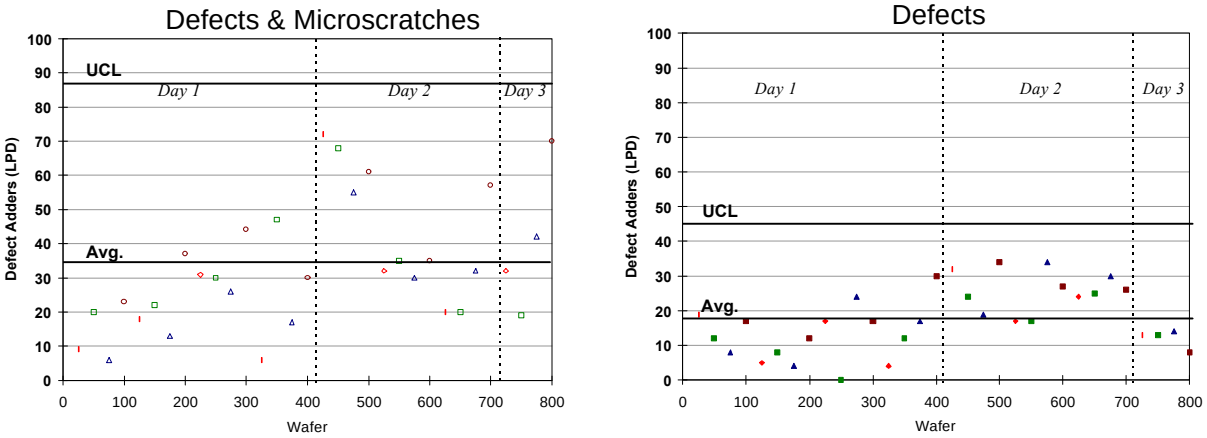

Fig. 7. Defect and micro-scratch counts in an extended run over 3 days with on oxide wafers using AEP ring and a 2 platen polish process.

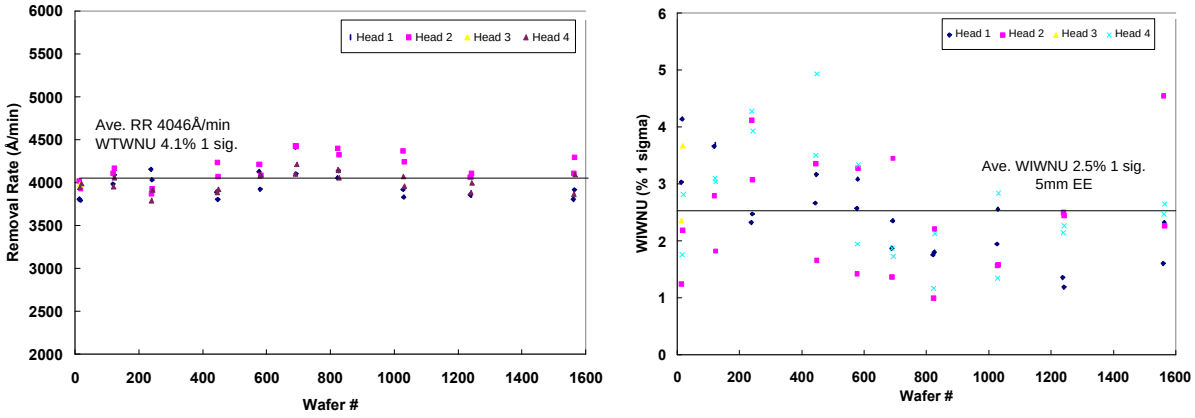

Fig. 8. An extended run using AEP ring with W wafers at 5 mm edge exclusion.

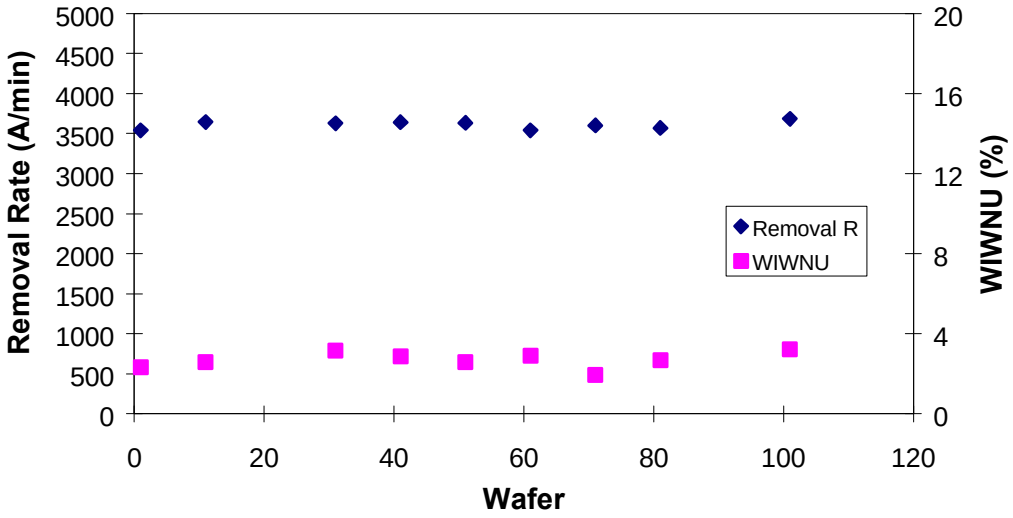

Fig. 9. An extended run using AEP ring with polysilicon wafers at 5 mm edge exclusion.