A Production-Proven Shallow Trench Isolation (STI) Solution Using Novel CMP Concepts*

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ABSTRACT

This paper reports advancement in STI CMP technologies developed on a new generation CMP tool. A STI solution based on new CMP concepts has been successfully implemented in an IC production fab for different devices (0.25μm and beyond) ranging from microprocessor to memory to analog devices having different pattern densities.

INTRODUCTION

In polysilicon CMP applications reported previously, dishing can be significantly reduced or completely eliminated by using a low- or no-selectivity slurry during over-polishing on a new generation CMP tool (a Mirra® CMP system) that features low removal rate within wafer non-uniformity (WIWNU).(1) Consistent low WIWNU and reliable end pointing using an ISRM™ end point system minimize polish-stopping-layer erosion. An new polishing head (Titan Head™) combined with consumable/process optimization improve WIWNU. All these approaches are also applicable to STI CMP applications. The STI CMP process developed using these approaches has been successfully implemented in an IC production fab.

STI CMP has been recognized as one of the most difficult CMP applications in IC fabrication. Planarity improvement has been one of the major topics under investigation to further advance STI CMP technologies. Because appropriate control experiments were not performed in a previous study, high speed was assumed to be responsible for better planarity achieved using a linear polisher.(2) In this work, we investigate the impact of pad and process variables on polishing planarity using a rotary CMP tool. The variables studied include pad type (solo vs. stacked), platen/head speed, and pressure. The experimental results showed that the hard solo pad was a dominant factor for achieving higher planarity. In the experimental ranges investigated, lower pressure led to higher planarity and planarity was insensitive to speed.

EXPERIMENTAL

A Mirra CMP system was used in this work for developing STI CMP processes and evaluating planarity. A modified MIT mask as described in a previous publication was used for STI evaluation.(3) The mask layout consists of 4x4 mm test structures with different percentage of active area ranging from 10% to 90% in each stepper field. Only 8” wafers were used for this work. Experimental descriptions for different experiments are included in the results and discussions section.

RESULTS AND DISCUSIONS

Impact of Slurry Selectivity on Dishing and Erosion

High selectivity slurry is commonly used in STI CMP to minimize nitride erosion. However, currently achievable selectivity necessitates device-layout design changes and is a strong function of pattern density. Selectivity varies from 85 (at 90% pattern density) to 25 (at 10% pattern density) for a widely used high-selectivity slurry as shown in Fig. 1. In addition, as shown in Fig. 2(left), the nitride pattern feature is rounded in the active areas where nitride has been exposed during over-polish.(3) Over-polish time has to be extended to completely remove oxide in the active areas if WIWNU is poor. The extended

over-polish time with a high selectivity slurry will unavoidably lead to more severe field oxide dishing as shown in Fig. 2(right). For a typical WIWNU, dishing is more pronounced when a high selectivity slurry is used as compared to a low selectivity slurry (Fig. 3). For example, after oxide removal in the active areas, dishing can be as deep as 1400Å on 1000µm-wide trenches when using a high selectivity slurry. In contrast, dishing can be less than 600Å (corresponding to <200Å nitride erosion) on 1000µm-wide trenches when using a low selectivity slurry. Severe dishing and the across wafer variation in dishing can lead to device failure. If dishing causes the field oxide recessing below the silicon surface prior to polysilicon deposition, polysilicon wrapping around the silicon device corner will result in higher sub-threshold leakage current.(4) Another potential device failure can be caused by polysilicon residues and/or stringers. The residues/stringers reside in the active areas and at the foot of the elevated field regions. The elevated field was created by high WIWNU or by large across wafer variation in dishing.

Minimization of Removal Rate Within Wafer Non-uniformity

It is critical to minimize WIWNU to reduce or eliminate dishing. In this work, low WIWNU was ensured mainly by integrating three approaches. The first approach was to employ a Titan Head. The Titan Head features a flexible membrane that applies uniform pressure on the wafer backside. A retaining ring with independent pressure control was used to adjust the removal rate at the edge of the wafer. The second approach was to optimize the process/consumable parameters. Low pressure (down to 2psi) and low selectivity slurry (e.g., colloidal SiO_2 slurry) were used to achieve a wider process window. Low WIWNU was achieved during trench oxide polishing by using the above two approaches as shown in Fig. 4. The third approach was to assure consistent end-pointing on nitride by utilizing a through-the-pad optical sensor. To demonstrate the insensitivity of end pointing to the deposited oxide thickness on incoming wafers, three STI wafers of different oxide thickness ranging from 6147Å to 12459Å were used. The pre- and post-CMP nitride thickness and oxide thickness were measured and compared to the actual end point time recorded by ISRM. The results are summarized in Table 1. The endpoint trace for each wafer is presented in Fig. 5. The results show that ISRM™ was insensitive to pre-CMP oxide thickness ranging from 6147Å to 12459Å. Consistent post-CMP thickness of nitride or oxide was achieved for wafers with a wide range of oxide thickness by reliably end pointing as evidenced in Table 1 and Fig. 5. As recorded in an IC production fab over three months, the ISRM end pointing had >99.9% success rate. By integrating the three aforementioned approaches, the WIWNU was kept less than 3% in a 360 wafer extended run (Fig. 6). Additionally, the post-CMP field oxide thickness was consistent across the extended run.

Minimization of Dishing and Erosion

Low WIWNU minimizes the need for over-polishing. Consistent end-pointing coupled with a low selectivity slurry and minimal over-polishing minimizes field oxide dishing and nitride erosion. Typical Mirra STI CMP performance is presented in Figs. 6-8. Fig. 6 shows that dishing as manifested by the remaining field or trench oxide thickness can be controlled. Fig. 7 shows that nitride erosion as manifested by post CMP nitride remaining thickness can be controlled to achieve nitride wafer-to-wafer non-uniformity (WTWNU) of 1.43% across a 100-wafer extended run. The remaining nitride thickness range (max-min) is controlled to less than 350Å with a 259Å average over the characterized features. Fig. 8 shows that both post CMP nitride and oxide thickness can be controlled during an optimized process run and a design-of-experiment (DOE) run. The post-CMP remaining oxide thickness is the difference between the deposited oxide thickness and the thickness removed. During the DOE, polishing rate was varied by changing pressure and platen/head rotation speed. However, the ISRM end point system coupled with an optimized process and Titan Head ensured consistent post CMP remaining nitride and oxide thickness. In this work, both SACVD oxide and HDP CVD oxide were used for trench fill. HDP CVD oxide fill showed a self-planarization effect due to sputtering during the deposition process. The self-planarization effect makes thinner trench oxide deposition practical and ultimately enables higher throughput on deposition

tools.(3) Nevertheless, oxide dishing and nitride erosion can be consistently controlled to a minimum for both SACVD and HDP CVD oxide trench fill as shown in Fig. 9.

This STI CMP process has been developed by minimizing dishing, erosion, and WIWNU and by utilizing low selectivity slurry. It was proven in a IC production fab that this process can be used for different devices (0.25µm and beyond) of different pattern densities without relying on typical integration solutions such as dummy features, reverse mask etch, blanket nitride film, thin nitride sandwich film. Dummy features not only increase photo mask fabrication expense, but also have a potentially negative impact on the devices, especially when a polysilicon capacitor design is used. Other integration solutions reported thus far increase manufacturing cost by introducing extra process steps. A STI CMP process without these integration expenses is very attractive to IC manufacturers.

Improvement of Planarity

Process and consumable parameters were investigated to improve planarity. The process parameters investigated are pressure (membrane, retaining ring and inner tube) and speed (platen and head). The consumable parameter investigated is pad type (IC1000 hard solo pad vs. IC1000/Suba IV stacked pad). The patterned wafers were prepared by depositing 16000Å PETEOS film for filling 8200Å deep trenches with different percentage of active area ranging from 10% to 90%. The mask used for wafer preparation has been described in the experimental section. For each experimental run, polishing time was controlled to remove 9000 +/- 500 Å PETEOS in the 50% active area. The results are presented in Fig. 10. The results show that the hard solo pad (IC1000) significantly improved planarity as compared the hard/soft stacked pad (IC1000/Suba IV) at both high speed (platen/head 153/147rpm) and low speed (platen/head 93/87rpm). By using a hard solo pad at low pressure (2/2.9/2 psi), the oxide thickness range (max-min) across the die with different percentage of active area was controlled within 1200Å which is about 1/3 of the typical range observed on the same test mask under the similar conditions when the hard/soft stacked pads were used. The three-fold planarity improvement achieved with a hard solo pad at low pressure (2/2.9/2 psi) was also supported by the planarization length calculated from this data at MIT. The planarization length with the stacked pad is about 6mm while planarization length of up to 15mm can be reached with a hard solo pad at similar conditions. A new model might be needed to prevent the underestimation of planarization length when a hard solo pad is used at low pressure or when the planarization length is above a certain value.(5) The irregular shape of the curves in Fig. 10 might be attributed to the influence of neighboring features with a very different percentage of active area. Influence by neighboring features is governed by mask layout. Lower pressure also improved the planarity as compared to high pressure in the tested range of 2/2.9/2 psi to 7/9/7 psi (membrane/retaining ring/inner tube) as shown in Fig. 11. The results indicate that planarity is insensitive to platen/head speed in the range of 93/87rpm to 153/147rpm on a 20” platen for both hard/soft stacked pads and a hard solo pad.

Notice that the planarization length calculated by the MIT group for this work on a Mirra system (6/15mm) is 100%/50% higher than that reported on different tools (3/9.5mm).(1) The planarization length was reported to be 3mm for a non-Mirra rotary tool and 9.5mm for a linear polisher with hard solo pad.(1) The improved planarity on the Mirra system was also observed in a separate tool-to-tool comparison study. In the tool comparison study, the planarization effect was evaluated by using similar consumable sets on five different CMP tools including the Mirra system. The actual polishing time was controlled on each individual CMP tool to achieve about 1000Å step height in the 500µm equal line/space area at the end of polishing. The post CMP polishing step height was plotted against the feature line width as shown in Fig. 12. The results show that the Mirra system is more effective in planarizing oxide in the feature size range from 500µm to 2000µm. The consistent step height (1000Å) across different features (from 500µm to 2000µm) can be achieved by timed polishing on the Mirra system. The remaining step heights after timed

polishing on other four CMP systems tested are sensitive to the feature sizes. The improved planarity on the Mirra system is attributed to Titan Head and an optimized process.

CONCLUSION

A robust STI CMP process has been developed and implemented in an IC production fab using a new generation CMP tool. The STI CMP process is based on the following concepts:

- low- or no-selectivity slurry for minimizing dishing during over-polishing,
- reliable ISRM end-pointing and consistent low WIWNU for minimizing nitride erosion,
- Titan Head with an optimized process/consumable-set for improving WIWNU and planarity.

The STI CMP process has been proven in IC production to be applicable to different devices (0.25µm and beyond) ranging from microprocessor to memory to analog devices of different pattern densities.

It was found that pad hardness is the dominant factor for achieving higher planarity. In the experimental ranges investigated, lower pressure led to higher planarity and planarity is insensitive to speed. A STI CMP process on a Mirra system using a hard solo pad at low pressure showed planarity 50% better than that achieved on a linear polisher and three-fold better than that achieved when hard solo pad is not used.

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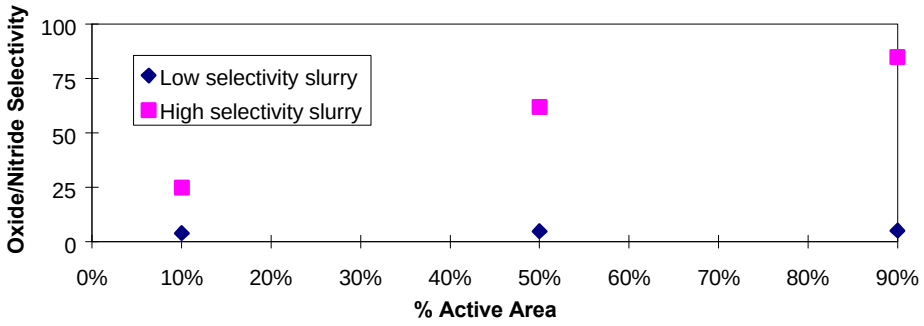

Fig. 1. Oxide/nitride selectivity as a function of the percentage of active area.

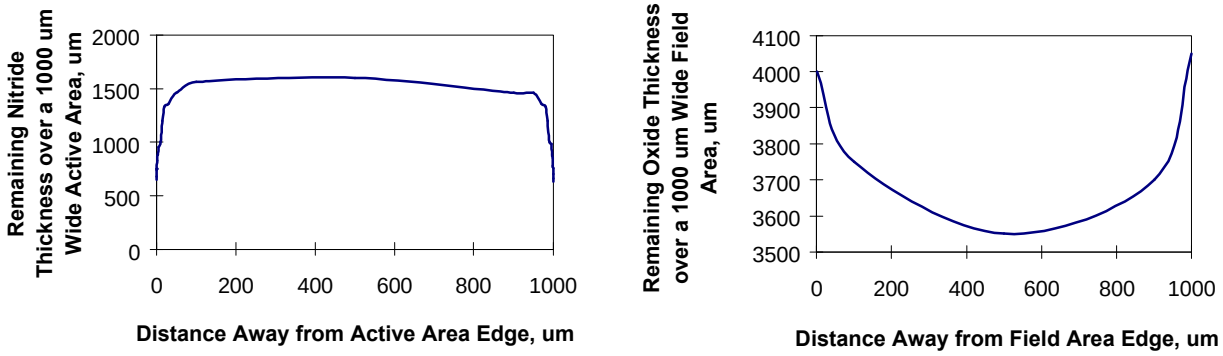

Fig. 2. Nitride erosion (left) and oxide dishing (right) in the 50% active area region of 1000µm feature size of equal line and equal space.

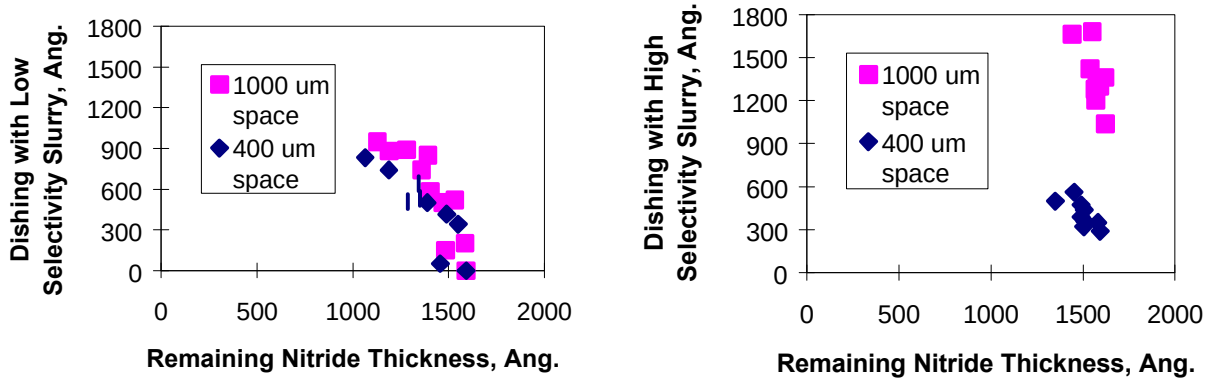

Fig. 3. Dishing as a function of slurry selectivity and over-polishing.

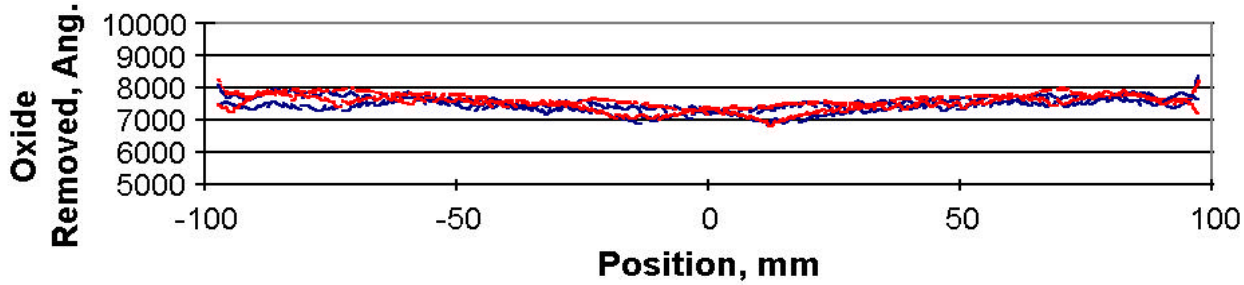

Fig. 4. Wafer diameter scans at 3mm edge exclusion on different polishing heads.

Table 1. Insensitivity of end pointing to the deposited oxide thickness on incoming STI wafers.

	Pre - CMP			Post - CMP	
Wafer No.	SiN Thick-ness (Å)	Deposited Oxide Thickness (Å)	CMP Time (sec)	Average Nitride Remaining in Active Region (A)	Average Oxide Thickness in Trench Region (A)
KC10AHG	1823	6147	121	1304	4514
KWA44XG	1842	9374	179	1281	4657
K70Q8GG	1909	12459	248	1429	4874

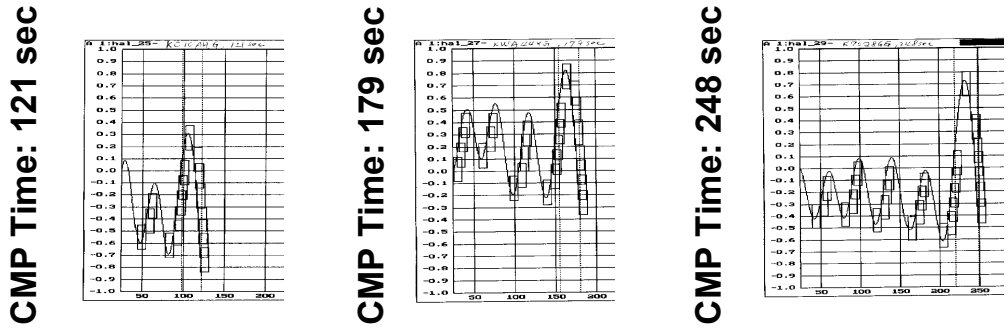

Fig. 5. End point trace for each of three patterned STI wafers described in Table 1.

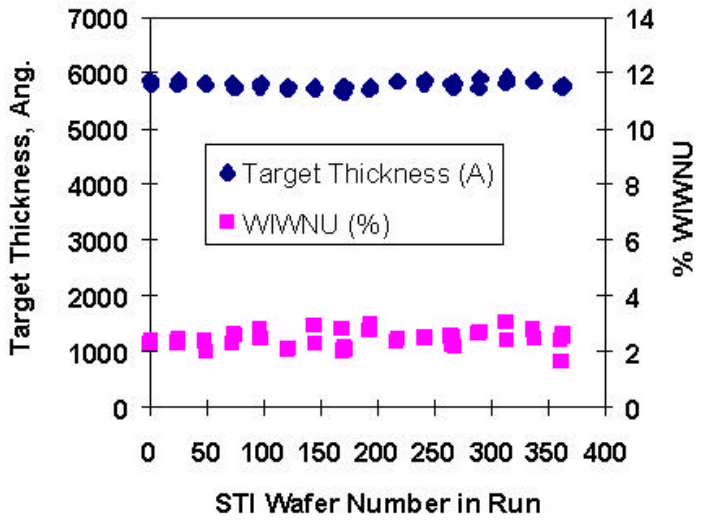

Fig. 6. Field oxide thickness and WIWNU as a function of wafer number in an extended run. Pressure (psi): 2.5/3/2.5 membrane/retaining-ring/inner tube. Speed (rpm): 63/57 platen/head. Pad: stacked IC1000/Suba IV.

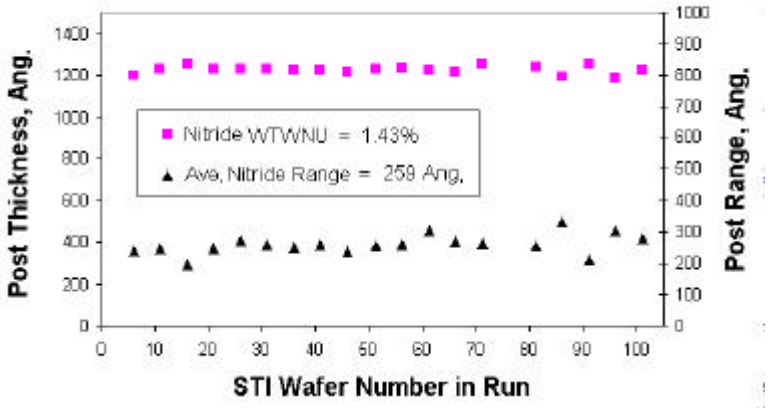

Fig. 7. Remaining nitride thickness and nitride thickness range (max-min) as a function of wafer number in an extended run. Pressure (psi): 4/4.6/4 membrane/retaining-ring/inner tube. Speed (rpm): 93/87 platen/head. Pad: stacked IC1000/Suba IV.

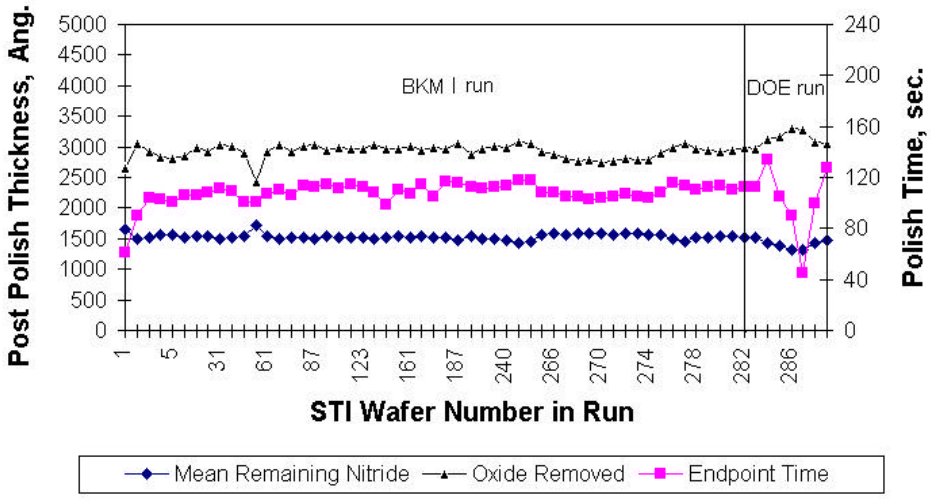

Fig. 8. Remaining nitride thickness, field oxide thickness, and actual polishing time at the end point as a function of wafer number in an extended run. Pressure (psi): 4/4.6/4 membrane/retaining-ring/inner tube. Speed (rpm): 63/57 platen/head. Pad: stacked IC1000/Suba IV.

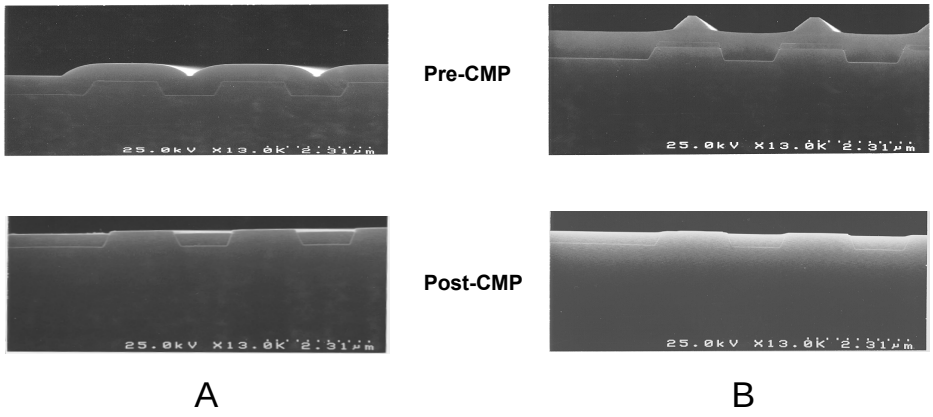

Fig. 9. Pre- and Post-CMP cross-section SEM micro-graphs for (A) SACVD oxide fill and (B) HDP CVD oxide fill.

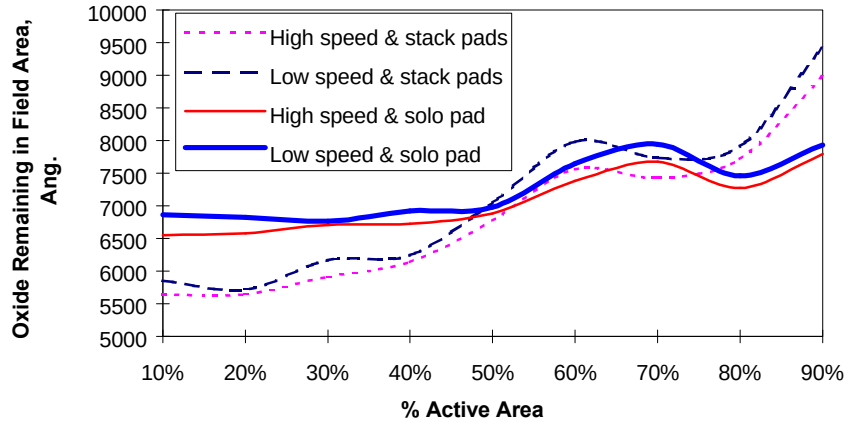

Fig. 10. Oxide remaining in the field area as a function of the percentage of active area after adjusted timed polishing.

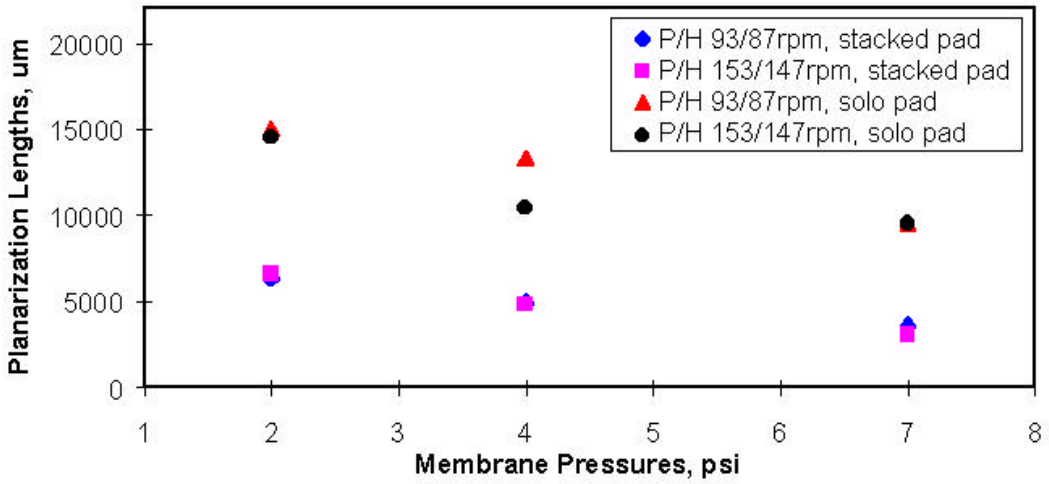

Fig. 11. Planarization length as a function of membrane pressure.

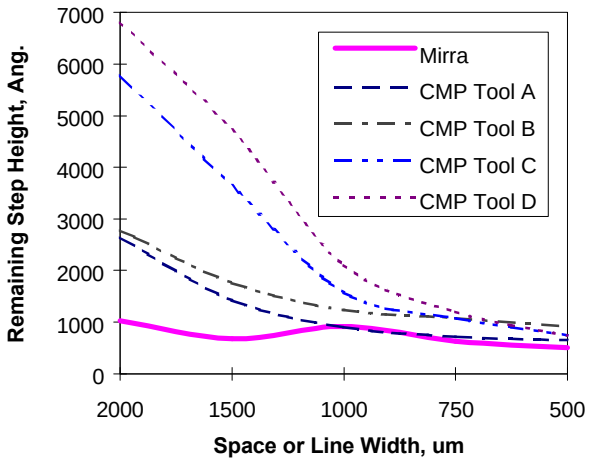

Fig. 12. Remaining oxide step height as a function of the line/space width.

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