ADVANCED FRONT END CMP AND INTEGRATION SOLUTIONS

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ABSTRACT

This paper will review and report significant advances in front end CMP and integration solutions that can be used for future IC devices. In order to increase tool availability and fab operation efficiency, a one-tool-for-all-application approach is used. In addition, these methods are compared to the capability of a next generation web tool with slurry-free polishing. The CMP technologies that are required for future generation devices include an advanced polishing head, an advanced in-situ endpoint system, and multi-platen, multi-head architecture. Coupling these hardware elements with next generation consumables, (solo hard pad, high planarity slurry, slurry-free polishing) enables direct polish STI process solutions that meet device requirements for 0.18µm and beyond. Polysilicon CMP is accomplished using a novel multi-step process. An advanced PMD process is demonstrated that exhibits a longer life pad and an advanced diamond disk for high throughput and high tool-availability. All the technologies have been successfully used or are currently being tested in production.

INTRODUCTION

Aggressive reductions in gate width and film thickness demand high performance and reliable front end CMP processes and hardware. Today, front end CMP consists mainly of STI (shallow trench isolation), polysilicon (i.e., Poly), and PMD (poly metal dielectric) CMP. To maximize the tool utilization and optimize the fab operation, IC manufacturers are asking the tool suppliers to offer the production proven tool for all three applications on a single tool. In this paper, recent advancements in STI, Poly and PMD CMP and integration solutions (including slurry-free polishing) will be presented.

EXPERIMENTAL

A stand-alone Mirra® CMP system with patented 4-head and 3-platen architecture or an integrated dry-in/dry-out Mirra Mesa™ system was used [1-2]. A modified MIT mask described in previous publication was used for STI process development [3]. Different pads (Rodel's k-grooved IC1000/Suba IV stacked pad, solo IC1000 hard pad without Suba IV sub pad, UR-100 pad, advanced longer life IC1010 pad) were used in process developments [3-5]. Rodel's Politex pad was used when buff was applied. The fixed abrasive pad by 3M was used for slurry-free polishing on Applied Materials' web technology tool. Cabot's SS-12 slurry was used in two STI processes (endpoint and low selectivity slurry process and solo hard pad process). Advanced CeO_2 slurry with additives by Hitachi Chemical was used in another STI process (advanced CeO_2 slurry process). Rodel's Advansil 2000 slurry was used for oxide breakthrough and poly overpolish [5]. Cabot's EP-P1000 slurry was used for poly main polish. For conditioning IC1000 or IC1010 pads, an improved diamond disk manufactured by Abrasive Technology using a high temperature Ni-Cr brazing process was used in conjunction with an advanced conditioner head assembly design. Poly wafers for extended runs were prepared by depositing 5000 Å undoped poly blanket film on top of 1000 Å thermal oxide substrate. BPSG wafers for extended runs were prepared in a SACVD™ chamber on the Producer™ platform. The BPSG film contains 5% boron and 5% phosphorus, both by weight.

RESULTS AND DISCUSSION

STI Process and Integration Solutions

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Endpoint and low selectivity slurry process

An ISRM^{TM} endpoint system was used for reliable endpointing on patterned wafers throughout this work [6]. The ISRM system is a laser based in-situ endpoint system sampling a center portion of the wafer. The ISRM system has been successfully used in volume production to eliminate rework due to underpolishing and scrap due to overpolishing. As shown in Fig.1, step height can be reduced to zero or near zero with ISRM and controlled over-polish [3]. Compared to SACVD, HDPCVD dielectric film provides wider process window possibly due to its hardness and its self-planarization effect. Nevertheless, ISRM endpointing and Titan Head^{TM} wafer carrier design enable Mirra platform as a drop-in tool to meet the requirements of advanced devices when SACVD or HDPCVD is used [7]. The cross section SEM micro-graphs of SACVD dielectric film prior to CMP and after CMP are included in Fig. 1. Non- or low-selectivity slurry ensures minimum field oxide dishing [8]. SS-12 slurry with oxide/nitride selectivity 3-4 : 1 was used in one of our released endpoint and low selectivity processes. Typical extended run performance of endpoint and low selectivity slurry process using STI wafers is presented in Fig. 2. Stable post-CMP field-oxide thickness was achieved over a 350-wafer marathon run. The average within-wafer non-uniformity (WIWNU) was 1.08% and wafer-to-wafer non-uniformity (WTWNU) was 2.40% over the marathon run. The same site of different dies for each wafer was measured to determine the post-CMP field-oxide thickness and non-uniformity.

Solo hard pad process

Many IC manufacturers are looking for direct STI solution without reverse mask etch steps. Improved planarity across different densities sand features is required for direct STI CMP. Utilization of a solo hard pad and low pressure significantly improves STI CMP planarity as shown in Fig. 3. The results also illustrate that planarity is independent of speed in the range of 243 to 400 ft/min [3]. The most commonly used speed in both linear and rotary polishers is in this range [9]. The potential positive impact of higher speed is the increased removal rate and hence higher throughput, which can be achieved by both linear and rotary polishers. As compared to a stacked pad, a solo hard pad increases planarity by a factor of 3 as shown in Fig. 3. Planarization length as modeled by the MIT group was increased from about 5 to 15mm at a low pressure when a solo hard pad was used. The field oxide remaining range in a wide active area range (10-90% on a modified MIT mask) was reduced from about 3600 to 1200 Å with a solo hard pad [8]. An optimized solo hard pad process has been recently developed to achieve a low WIWNU (average <3%) and a stable removal rate (>2600 Å/min) during a more than 900-wafer marathon run [10]. Low defect and micro-scratch counts (average <50) was also achieved during the marathon run. Feasibility of solo hard pad process has been shown to widen direct STI polish process window.

Advanced CeO_2 slurry process

An advanced CeO_2 slurry with additives was developed in Japan. It contains about 5% CeO_2 abrasive in a weak alkaline (pH 8.3) aqueous media [11]. The process developed on the Mirra platform using the advanced slurry has demonstrated that field oxide dishing can be significantly reduced as compared to a SiO_2 slurry process. An advanced slurry offers reduced dishing at a higher additive concentration and improved polishing rate at a lower additive concentration. Advanced CeO_2 slurry process leads to uniform field oxide range across different densities as shown on the modified MIT mask [10]. Typical polishing performance using an advanced slurry process is presented in Fig. 4. Relative field oxide thickness before and after CMP is plotted against the position across the wafer in Fig. 4(A). The results show that average removal rates at different positions across the wafer are consistent [3] The process offers high oxide/nitride selectivity. At the end of the CMP process, less than 10% of nitride film was eroded as shown in Fig. 4(B). The advanced CeO_2 slurry process has demonstrated significant potential as a means of implementing direct polish STI for volume production.

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Slurry-free polishing process

The Slurry-free polishing process employs web technology and a fixed abrasive pad. This process does not require slurry feed but instead uses an aqueous chemical solution. The fixed abrasive pad consists of a micro-replicated abrasive layer, rigid layer, and resilient layer [12]. The Applied Materials' web technology enables pad incrementing for steady state conditions during polishing as shown schematically in Fig. 5. By using web technology, each wafer will see the same pad conditions. Pad life is de-coupled from polishing process. When applied to STI CMP, the slurry-free polishing process demonstrated significant potential to provide less dishing and uniform nitride thickness enabling direct polish STI as compared to conventional slurry polishing (Fig. 6). The cross section SEM micro-graphs shown that dishing over 0.25 µm trenches was negligible for slurry-free polishing, whereas dishing was significant for conventional slurry CMP. As compared to other polishers, Applied Materials' web platform with slurry-free polishing significantly reduced field oxide dishing down to less than 200 Å across the wafer as shown in Fig. 7 [13]. Defect reduction has been a major focus in an earlier development stage of the slurry-free polishing product. After several fixed abrasive pad revisions and subsequent process optimization, the defect and micro-scratch counts with slurry-free polishing is comparable to the conventional polishing [14]. Typical nitride erosion by slurry-free polishing is less than 300 Å as shown in Fig. 8.

Process performance comparison

Nitride erosion and oxide dishing performance of slurry-free polishing and other new processes developed or being developed at Applied Materials is compared to current process in Table 1. For convenience, dishing over a 100 µm trench was used for comparison. Obviously, dishing over narrower trenches is much less than the 100 µm trench. Table 1 shows all of the new processes on Applied Materials' platforms offer the improved oxide dishing and nitride erosion performance which enables a direct polish STI solution.

Poly Process and Integration Solutions

Many DRAM manufacturers and advanced analog manufacturers are using poly CMP in their fabs for new generation devices. The poly CMP process consists of multiple steps using two slurries: oxide breakthrough polish, poly main polish, endpoint, poly over-polish, and buffing and rinse. The Oxide breakthrough polish using non-selective slurry and the 1st part of poly main polish using a different high-removal rate, high-selectivity (poly/oxide) slurry was conducted on platen 1. Oxide breakthrough polish is critical to remove the layer of cap oxide for low WIWNU [5]. The poly main polish continues on platen 2 until the endpoint is reached. The process continues using the non-selective slurry for over-polishing, to minimize dishing. Once polishing is complete, a separate step on platen 3 cleans and re-oxidizes the poly surface to prevent dopant loss. By allowing sequential multi-step processing, the Mirra system maintains high throughput. Process performance in terms of removal rate, WIWNU and defects is summarized in Fig. 9. The results (Fig. 9A) show that Applied Materials' poly CMP process provides high stable removal rate (average 4467 Å/min) at a low WIWNU (average 1.8%) over a 1400-wafer marathon run. Low defect and micro-scratch counts (average <50) were achieved as shown in Fig. 9B. Both Si substrate (for > 0.16 µm particle) and SiO_2 substrate (for 0.2 and 0.25 µm particles) were used for particle monitor wafers to confirm low defect and micro-scratch counts. Increased defect counts starting from wafer # 400 in Fig. 9B is due to a known cause (i.e., a clean chemical component change) which can be easily corrected and prevented as shown in another extended run reported previously [5]. The average defect counts were less than 25 in the previous extended run.

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The poly CMP process has been successfully used at a number of advanced logic and DRAM fabs to form poly capacitor, gate and contacts in new generation devices. Poly plug formation is important to build storage cells in advanced DRAM devices. Poly CMP is a critical step in poly plug formation. As for other poly CMP applications, successful poly CMP in poly plug formation requires reliable endpoint, low WIWNU, high planarity, minimum dishing, low defects, and negligible dopant escape for doped poly. The ISRM endpoint system controls over-polishing to minimize oxide erosion and poly dishing effects. It accurately identifies the point at which the poly has been completely removed to end polishing, thereby limiting the loss of poly in the plug, contacts and trenches. Given the high selectivity of slurry and the accuracy of ISRM endpointing, the need for a typical sacrificial nitride stop layer can be eliminated, offering a simplified and lower cost production process.

Many process integration approaches have been made after employing advanced poly CMP technology [15-16]. Dual poly damascene for poly gate and self aligned poly contact formation employs two poly CMP runs following an advanced STI CMP as shown schematically in Fig. 10A. In this integration approach, uniform thick nitride remaining after STI CMP is important [14]. Following STI formation, a trench was formed in nitride film by lithography and then plasma etching before stopping on Si. The process flow continues with gate oxide formation and then poly deposition followed by the 1st poly CMP run. After this 1st poly damascene, spacer and contact holes are formed after removing remaining nitride. The 2nd poly damascene is completed after poly deposition and then another poly CMP run. To make this integration approach successful, both advanced poly CMP and advanced STI CMP processes are critical. This integration approach has potential to solve five major front end integration problems:

- contact etch stopping on poly gate while forming contact holes exposing source/drain area,
- minimize/eliminate plasma damaging on gate oxide,
- shrink die size by forming SAC -- self-aligned contact,
- control contact CD – critical dimension,
- dual salicide for low contact resistance and low poly gate sheet resistance.

Overall, this approach has the potential to shrink gate width down to 0.07u and below with smaller die size. It could maintain good junction integrity after subsequent contact etching and metallization processes for advanced devices [15].

Another integration approach with poly CMP step uses the self-aligned metal gate (SAMG) Cloisonne process as shown schematically in Fig.10B. The integration approach starts with oxide deposition after STI, poly gate, and spacer formation. The process flow continues with poly CMP after oxide CMP to expose poly gate across the wafer. Then, top portion of poly gate is removed using selective plasma etch. Metal gate is formed by metal deposition followed by metal CMP. The feasibility of this integration approach has been successfully demonstrated to aid advancing device technology by reducing gate sheet resistance (Ro < 1) [16].

PMD Process Solutions

A major focus for PMD CMP has been on improving pad life, reducing cost of consumables (CoC), increasing tool availability, and further improving polishing performance (low defects, high planarity, low WIWNU, and high stable removal rate). Significant progress has been made on all fronts over the last two years. An advanced longer life IC1010 pad has been developed and implemented in volume production [4]. Typical extended run results on BPSG dielectric films are shown in Fig. 11. High removal rate (average >4900 Å/min), low within-wafer WIWNU (average < 3%), and low defect counts (average < 22) were achieved over a more than 1200-wafer marathon run. This extended run was stopped due to the tool allocation for other experiments. Much longer pad life is expected from the pad based on the significant amount of groove depth left at the end of run. As demonstrated by 7 extended runs on BPSG films and14 extended runs on thermal oxide films in the application lab and field data from three different customer

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sites, the IC1010 pad at least doubled pad life as compared to the IC1000 pad. Planarity performance for the IC1010 pad is comparable to performance obtained using the IC1000 pad [4]. Longer pad life and comparable or improved polishing performance achieved using IC1010 pad process are attributed mainly to the following factors:

1) larger and more consistent pad grooves,
2) uniform pad wear using an advanced conditioning disk [17],
3) uniform transportation of slurry and polishing by-products to and from polishing zone, and
4) uniform temperature distribution on the wafer and pad in the polishing zone during polishing.

Longer pad life can translate into lower CoO (cost of ownership). Longer pad life also increases CMP tool availability and wafer output (wafer starts per week) at any given wafer throughput (wafers per hour) [4]. Planarity improvement achieved in STI development has also been successfully implemented in the PMD application, both in the lab and in volume production.

Front End CMP Integrations

New hardware, consumable sets, and processes developed initially for a specific front end application described in this paper (STI, poly, PMD) have been found to be applicable to other applications. Since all three front end CMP applications (STI, poly and PMD) do not expose metal films to the polishing system, it is relatively easy to switch from one application to another on the same tool as far as metal ion contamination is concerned. When different consumable sets are used for different applications, a switch to the specific consumable set for the specific application is necessary. The Mirra platform offers multiple slurries for each platen with the ability to purge and switch when changing applications. The switch will be automatic when proper slurries are connected to the specific platen. All polishing parameters (e.g., pressure, speed, endpoint recipe, etc.) can be automatically down-loaded along with a process recipe for each CMP application. A CMP tool being used for all applications and backing up another tool gives R&D, pilot line and large volume production fabs significant leeway to increase fab operation efficiency. Several advanced IC fabs have successfully adapted this one-tool-for-all-application approach in their front end volume production.

CONCLUSIONS

The Mirra platform has proven to be a reliable CMP tool for all three front end applications (STI, poly, PMD) in volume production of advanced IC devices. A process switch between any two of the three front end CMP applications can be conducted on the same Mirra CMP tool. This one-tool-for-all-application approach has been successfully practiced in the front end of volume production to facilitate the tool backing up each other and to increase tool availability and fab operation efficiency. Significant advances of front end CMP technologies have been achieved for future generation devices.

Four different STI CMP solutions have been developed and are being advanced. Endpoint and low selectivity STI CMP process has been successfully used in volume production. Three new STI CMP technologies (solo hard pad, high planarity slurry, slurry-free polishing) have shown significantly improved planarity. Slurry-free polishing using Applied Materials' web technology improved field oxide dishing by more than 80% and reduced nitride erosion by more than 40% as compared to current process. Advanced poly CMP process has proven to be important in many emerging device technologies. A two-slurry and multiple-step poly CMP process showed high stable removal rate at a low WIWNU and low defect and micro-scratch counts. An IC1010 pad process using advanced conditioning disk has proven to be successful for PMD CMP and other applications in both R&D lab and volume production fab. The process doubles pad life and significantly reduces CoO by increasing CMP tool availability and wafer output. All the new technologies developed for one application can be potentially used for other front end applications.

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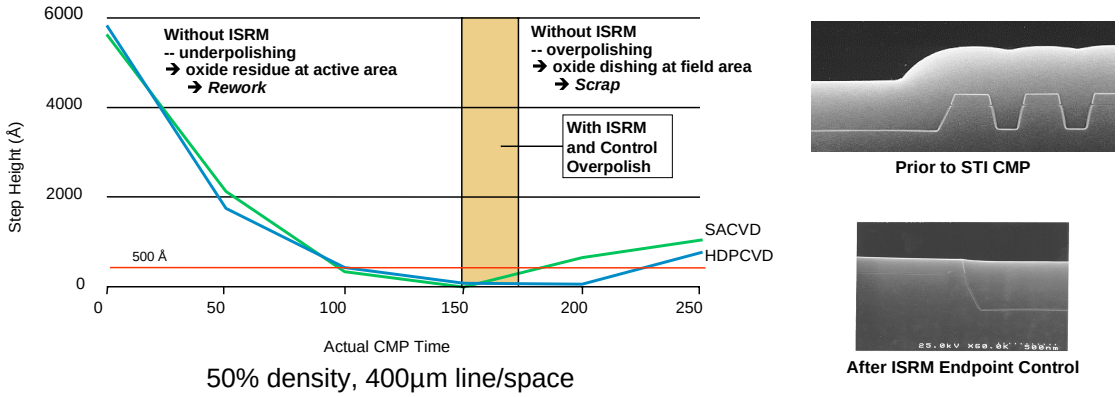

Fig. 1. Step height as a function of polishing time for two different types of oxide films (HDPCVD and SACVD) with and without ISRM endpoint system control [3].

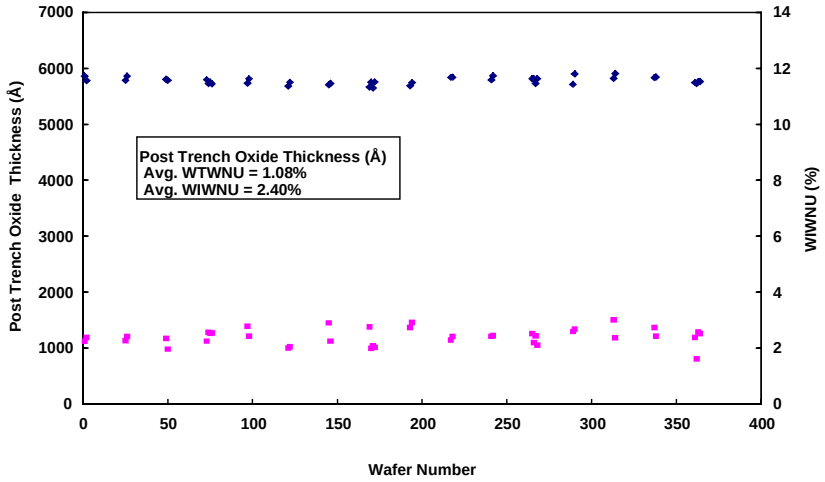

Fig. 2. An extended run of STI wafer polishing using an endpoint and low selectivity slurry process. (Information presented with customer permission.)

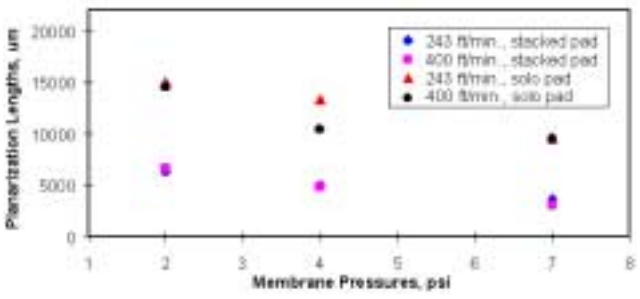

Fig. 3A. The impact of pad hardness, polishing pressure, and speed on modeled planarization length [3].

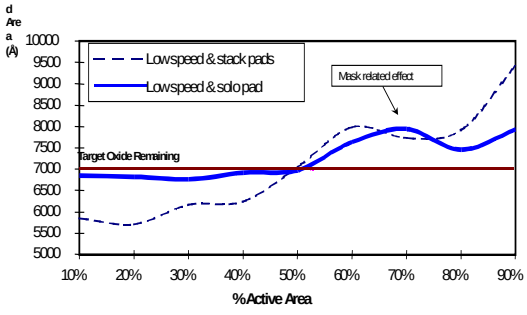

Fig. 3B. The impact of pad hardness and polishing pressure on the step height range across 10-90% active area recorded after removing 9000Å oxide at 50% density structure [3]

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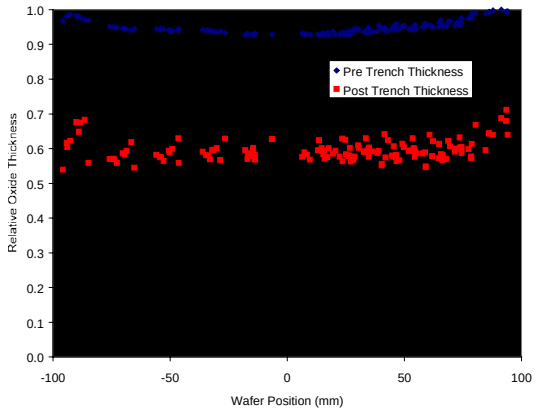

Fig. 4A. Trench oxide thickness before and after CMP as a function of the testing site position on a wafer [3].

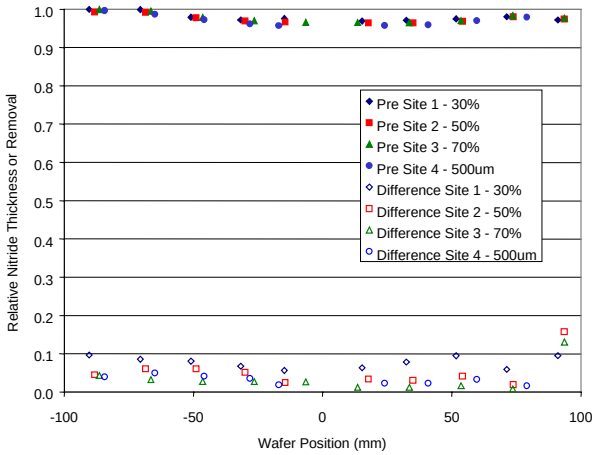

Fig. 4B. Nitride erosion at different density structures and features as a function of the testing site position on a wafer [3].

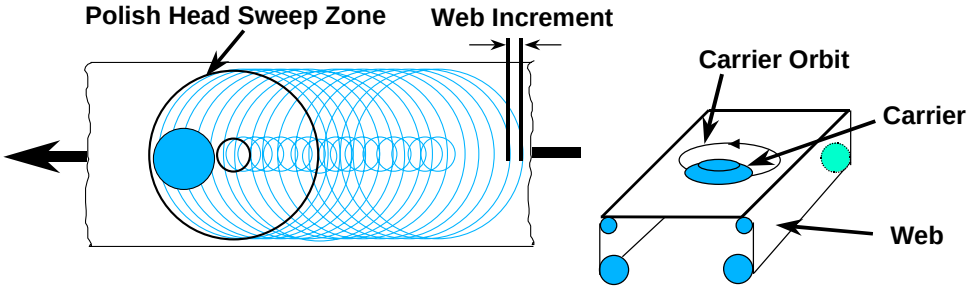

Fig. 5. A schematic diagram of Applied Materials' web technology.

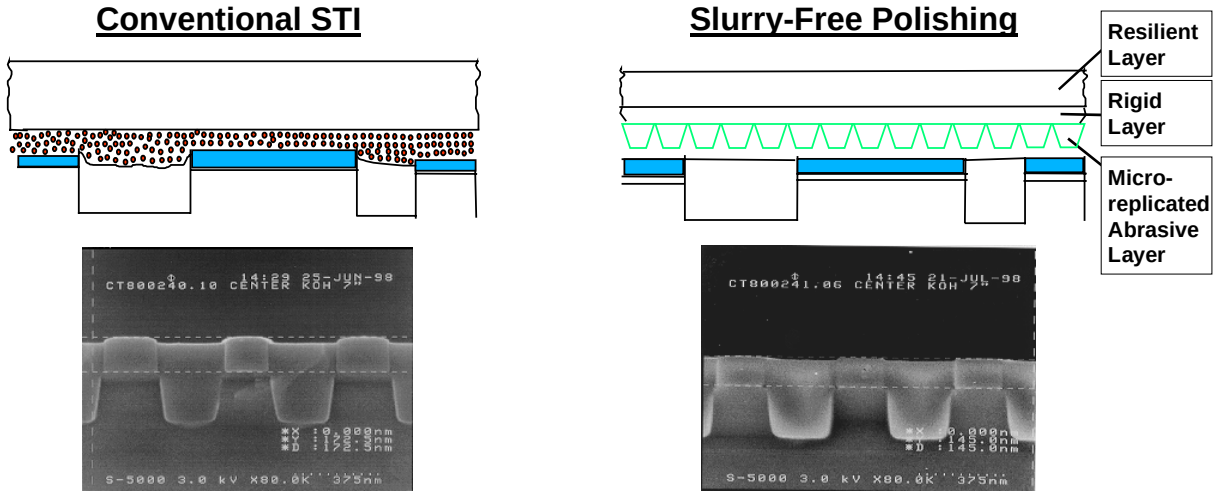

Fig. 6. A schematic diagram and cross section SEM micro-graphs of STI slurry-free polishing compared to conventional slurry CMP process. (SEM pictures presented with customer permission.)

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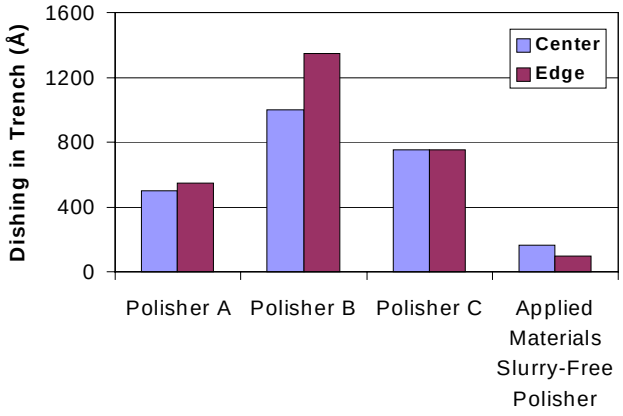

Fig. 7. Field oxide dishing over 100 µm trench of Applied Materials' slurry-free polishing platform as compared to three other different polishers using slurries. (Information presented with customer permission.)

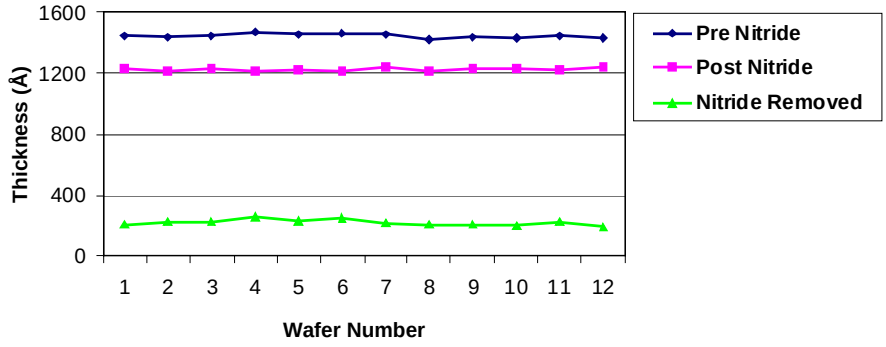

Fig. 8. Nitride erosion performance of slurry-free polishing. (Information presented with customer permission.)

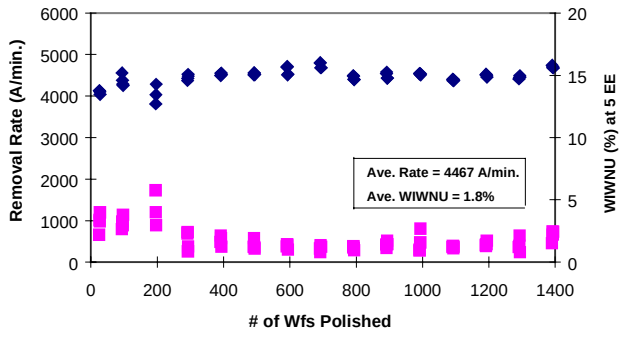

Fig. 9A. Poly removal rate and WIWNU as a function of wafer number in an extended run using Applied Materials process.

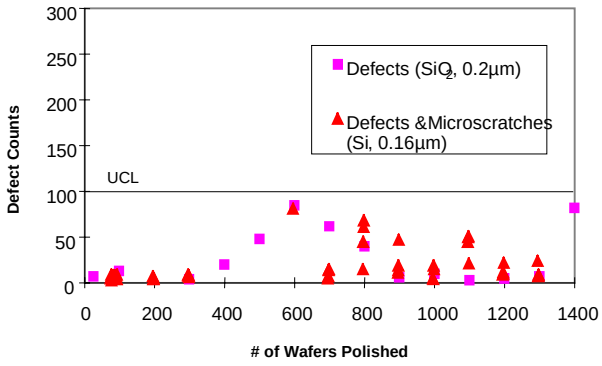

Fig. 9B. Defect and micro-scratch counts as a function of wafer number in an extended run using Applied Materials process.

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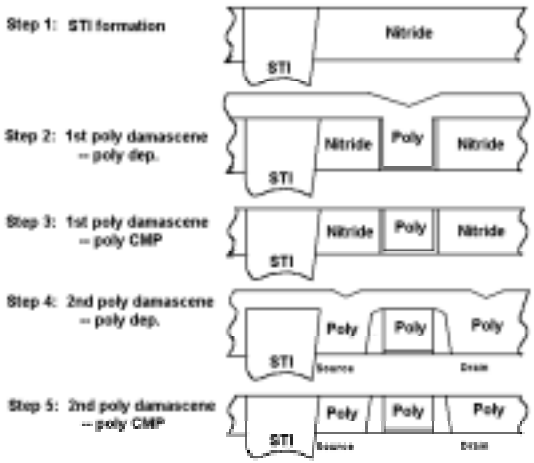

Fig. 10A. A schematic diagram of dual poly damascene for poly gate and self aligned poly contact formation.

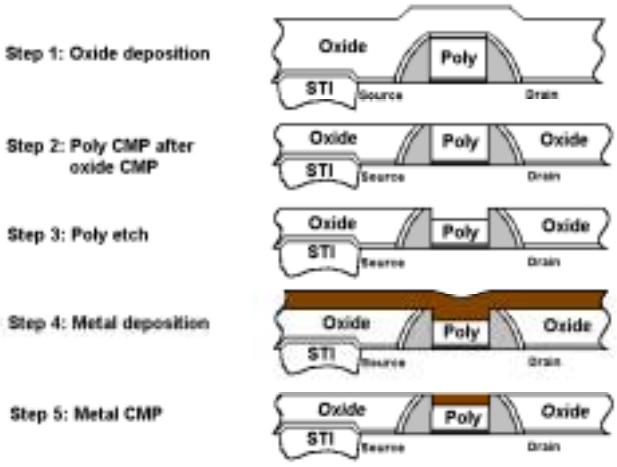

Fig. 10B. A schematic diagram of self aligned metal gate Cloisonne process [5].

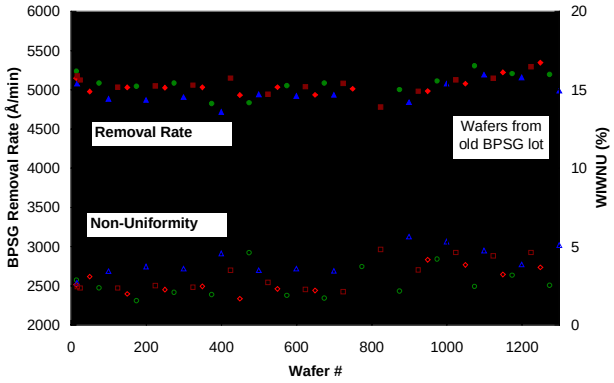

Fig. 11A. Oxide removal rate and WIWNU in an IC1010 pad extended run using BPSG wafers.

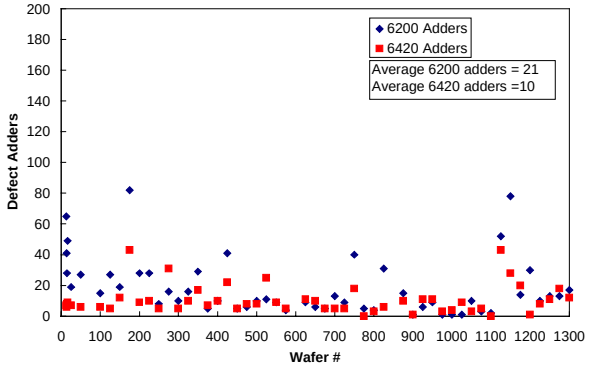

Fig. 11B. Defect counts (SS6200 and SS6420 adders) in an IC1010 pad extended run.

Table 1. Nitride erosion and field oxide dishing performance comparison. (Slurry-free polishing information presented with customer permission.)

	Nitride Loss, Å (*reduction in % wrt. baseline*)	**Dishing at 100 µm trench, Å** (*reduction in % wrt. baseline*)
Current baseline, In volume production	500	1200
IC1010 w/ Suba IV at low pressure	350 (*30%*)	700 (*42%*)
IC1010 solo pad at low pressure	250 (*50%*)	500 (*58%*)
Advanced slurry with IC1000 pad	150 (*70%*)	300 (*75%*)
Slurry-free polishing with FA pad	<300 (*40%*)	<200 (*83%*)

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