# Adcon® Wafer Highlights

- Adcon offers full ranges of standard and application-specific patterned, blanket film, and substrate wafers for your CMP and cleaning product R&D needs in both IC and solar industries
- Adcon offers up to 30% discount for the products equivalent to or better than the products from other suppliers; Adcon provides a variety of free and world-class professional services for the same or superior quality products and the same price as other suppliers
- Adcon forms partnership with multiple foundries (including both multi-billion-$ leading semiconductor manufacturers capable of manufacturing patterned wafers of sub-65nm technology nodes and leading solar cell manufacturers) to design and manufacture advanced and mainstream IC device wafers, patterned wafers, film/film-stack wafers, and solar wafers/cells. When requested, Adcon guarantees that Adcon wafers are identical to industry standard wafers in terms of mask layout and manufacturing methods and exceeding the standard wafers in terms of product quality and customer services.

# Cu Wafers and Electrical Tests

- Cu interconnect patterned or IC device wafers: oxide, different low k dielectric (including Black Diamond, Coral, FSG and others), different wafer sizes (including 200mm & 300mm), different technology nodes (0.25um to 65nm and beyond), any masks (standard MIT/Sematech masks including 854 or other test or IC device masks, including SRAM or other memories or mainstream logic), single damascene, dual damascene, standard or customer designs, short/long/full loops
- Pre-measured (for defects) electrical testable or IC device wafers (with or without functional transistors) for post CMP and/or post cleaning evaluations (defects or yield inspected by different metrology tools, including KLA2139, AIT, ES20, and electrical testers), as compared to baseline or industry benchmarks
- Different low k dielectric (Black Diamond, Coral, FSG and others) or Cu/Ta or Cu/TaN or thick Ta or TaN blanket film wafers (on different wafer fab equipments by different manufacturers) of different film thickness, different film stacks, different defect grades, and different wafer sizes (including 200mm & 300mm)

# STI Wafers and Electrical Tests

- STI patterned or IC device wafers with different trench oxide (HDPCVD & SACVD), different wafer sizes (including 200mm & 300mm), different technology nodes (0.5um to 65nm and beyond), any masks (standard MIT/Sematech masks including 864 or other test masks or IC device masks, including SRAM or other memories or mainstream logic), customer designed unique trench depth or oxide overburden thickness, short/long/full loops. Choices of standard design and recyclable advanced designs for half of the unit price, as compared to industry benchmarks
- Pre-measured (for defects) electrical testable or IC device wafers (with or without functional transistors) for post CMP and/or post cleaning evaluations (defects or yield inspected by different metrology tools, including KLA2139, AIT, and electrical testers), as compared to baseline or industry benchmarks
- Different oxide (HDPCVD, SACVD, PECVD Teos, Thermal oxide, and others, on different wafer fab equipments by different manufacturers) or nitride blanket film wafers of different film thickness, different defect grades, and different wafer sizes (including 200mm & 300mm)

# W Wafers and Electrical Tests

- W Contact and VIA patterned or IC device wafers, different wafer sizes (including 200mm & 300mm), different technology nodes (0.5um to 65nm and beyond), any masks (standard MIT/Sematech masks or other test masks or IC device masks, including SRAM or other memories or mainstream logic), standard or customer designed contact/VIA/trench depth or W overburden thickness, standard or customer designs, short/long/full loops.
- Pre-measured (for defects) electrical testable or IC device wafers (with or without functional transistors) for post CMP and/or post cleaning evaluations (defects or yield inspected by different metrology tools, including KLA2139, AIT, ES20, and electrical testers), as compared to baseline or industry benchmarks
- W blanket film wafers of different film thickness and different glue (Ti/TiN, Ti/TiW) layers, thick Ti/TiN, Ti/TiW, Ti blanket film wafers (on different wafer fab equipments by different manufacturers) of different film thickness, different defect grades, and different wafer sizes (including 200mm & 300mm)

# Polysilicon Wafers and Electrical Tests

- Polysilicon (blanket film stack or patterned or IC device) wafers:
  - Different polysilicon: undoped crystalline, doped crystalline, undoped amorphous Si, doped amorphous Si, different dopants and dopant concentrations
  - Different patterned polysilicon wafers (trench or plug, polysilicon capacitor or polysilicon gate or other advanced applications) and IC device wafers
  - Different trench or plug depth and polysilicon overburden thickness
  - Different masks, standard masks or other masks used in IC fabs
  - Different wafer sizes (including 200mm & 300mm) and different technology nodes (0.5um to 65nm and beyond)
- Pre-measured (for defects) electrical testable or IC device wafers (with or without functional transistors) for post CMP and/or post cleaning evaluations (defects or yield inspected by different metrology tools, including KLA2139, AIT, and electrical testers), as compared to baseline or industry benchmarks

# PMD/ILD Wafers and Electrical Tests

- PMD/ILD patterned or IC device wafers with different dielectrics and different technology nodes (0.5um to sub-65nm), different wafer sizes (including 200mm & 300mm), any masks (standard masks or other test masks or IC device masks, including SRAM or other memories or mainstream logic), standard or customer designed trench depth or oxide overburden thickness, standard or customer designs, short/long/full loops
- Pre-measured (for defects) electrical testable or IC device wafers (with or without functional transistors) for post CMP and/or post cleaning evaluations (defects or yield inspected by different metrology tools, including KLA2139, AIT, and electrical testers), as compared to baseline or industry benchmarks
- Different oxide or other dielectric blanket film wafers of different film thickness and different defect grades, on different wafer fab equipments by different manufacturers

# High k and Metal Gates Wafers

- $HfO_2$, $HfSiO_2$, HfZrOx, $ZrO_2$, $ZrSiO_2$ films
- HfN, HfON, HfSiN, HfSiON, ZrN, ZrSiN, ZrON, ZrSiON films
- TiO, TaO, TaSiO, TiSiO films
- $Al_2O_3$, $Ta_2O_5$, $La_2O_3$, $TiO_3$ films
- Ti, Ta, TaN, TiN, Al, W films
- Specifically designed patterned wafers for developing high-k/metal-gate process module
- Electrical parameter and sort yield or failure analyses for process module development and integration optimization, demonstrating the superiority of your own CMP/cleaning consumables or equipments over industry benchmarks when applied to high k and metal gate test wafers

# Wafers with Noble Metals & Other New Materials/Designs

- Ir, Ru, Pt, Pd, NiFe, Charcogenide blanket films or their patterned wafers for MRAM, phase change memory, advanced DRAM or other new devices (different technology nodes, different wafer sizes, any masks, short/long/full loops)
- Thick or ALD barrier films
- Co or Co alloy for low k dielectric cap
- CMP/clean test wafers with customer specific TSV process flow
- Specifically designed wafers for fixed abrasive pad conditioning or polishing pad break-in
- Electrical parameter and sort yield or failure analyses for process module development and integration optimization, demonstrating the superiority of your own CMP/cleaning consumables or equipments over industry benchmarks when applied to the test wafers that employ new materials and/or designs

# Wafers for Post Plasma Etch/ Ash or Post CMP Cleaning

- Different patterned or film/film-stack or IC device wafers (single or dual damascene Cu/low k, high k, metal gate, STI, W, polysilicon, oxide or PMD/ILD) for cleaning solution or striper evaluation (post plasma etch or post ash or post CMP, per customer's specific designs) at different technology nodes (0.5um to sub-65nm),
  - Post-VIA/contact etch (Cu/low k or Al interconnects, post-ash. Ta or Ta/TaN barriers, TiN liner, TiW liner. Underneath metal (Cu or Al) exposed. Verification of significant post-ash residue remaining)
  - Post-metal etch (Al interconnect, post-ash. Verification of significant post-ash residue remaining)
  - Post CMP wafers for different applications (single or dual damascene Cu/low k, high k, metal gate, STI, W, polysilicon, oxide or PMD/ILD)
- Electrical testable or IC device wafers (with or without functional transistors) for post CMP and/or post cleaning evaluations (defects or yield inspected by different metrology tools, including KLA2139, AIT, ES20, and electrical testers), as compared to baseline or industry benchmarks

# Wafer Substrates

- Different finishing, sampled at different stages of wafer substrate manufacturing:
  - Wafers before final polishing for developing final polishing slurry
  - Wafers before intermediate polishing for intermediate polishing slurry
  - Wafers before rough polishing for rough polishing slurry
  - Wafers before edge polishing for edge polishing slurry
  - Customer specific solar wafers (monocrystaline or polysilicon) of different size (125x125mm or 156x156mm) and thickness before or after texturing
- Bare silicon wafers of different diameters (300mm, 200mm, and smaller sizes), different substrates (Si & GaAs & Al2O3) and different grades (including prime grade wafer and different test grade wafers: Epi virgin Si, non-Epi virgin Si, reclaimed silicon wafers, and other sub-grades, related to particle counts and lithography needs, with different pre-measurement data files)

# Adcon® IC/Solar Fab Services

- Adcon and its business model enable you to become virtual IC/solar fab staffs to design, manufacture, and acquire all kinds of blanket films, patterned wafers, IC device wafers, and solar wafers/cells and to conduct critical experiments and product R&D and qualifications (short/long/full loop wafer splits) for your specific CMP and cleaning product development needs, without investing your own capitals and resources in purchasing and maintaining multi-million $ equipments and multi-billion $ IC/solar fabs
- There are no projects or programs too big or too small for our world-class professionals to help you achieving technology, financial, and business goals in this competitive market
- Adcon and its fab partners (including multi-billion-$ leading semiconductor and solar manufacturers capable of manufacturing patterned wafers of sub-65nm technology nodes and advanced solar cells) are ready to visit your facilities or invite your team to visit our world-class fab facilities to discuss and finalize your new R&D and product qualification needs