Advanced STI CMP Solutions for New Device Technologies

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Biography:
Jeffrey David received his B.S. in Electrical Engineering from Purdue University in 1996. From there he joined Applied Materials through the New College Graduate Training program, where he was trained on various Semiconductor processes and products at Applied Materials. Jeff has spent the last 2 1/2 years as a Process Engineer in the CMP division working on the Mirra® polishing system. His main focus recently has been Planarity and the STI process.

Benjamin A. Bonner received his B.S. in chemistry from Southwest Missouri State University and his M.S. in chemistry from The University of Arizona. His graduate work focused on synthetic polymer organic chemistry. He spent 3 years teaching chemistry at the college level. He has been a process engineer at Applied Materials CMP division for two years.

Thomas H. Osterheld received his B.S. in Chemistry from the University of Montana and his Ph.D. in Physical Chemistry from Stanford University. His graduate work focused on gas-phase ion chemistry. He spent 3 years at Sandia National Labs studying reaction mechanisms of high temperature CVD and CVI systems. He has been at Applied Materials for 4 years and currently manages the dielectric CMP process development group.

Raymond Jin was an honorary graduate from University of Utah with a Ph.D. in Metallurgy and Materials Science. He has 11 years of industrial experience as a technologist, program manager, section head/manager in CMP development, new material/chemical R&D, capital equipment selection, and 0.5u/0.35u/0.25u/0.18u/0.15u front/back end CMOS/BiCMOS process module development/integration/transferring. Prior to joining Applied Materials, he worked at National Semiconductor, Cypress Semiconductor and Pilkington. He currently manages strategic products including STI in the CMP Division at Applied Materials.

Abstract:
This paper reviews and reports advancements in developing STI CMP processes for new device technologies. Three major STI CMP processes developed on a Mirra® polishing system are discussed. Using patented multi-head and multi-platen architecture with the advanced Titan Head™ carrier and ISRM™ endpoint detection system, STI CMP has been successfully demonstrated in the volume production of various devices including analog, memory, and mixed signal devices. The first production-proven STI CMP process was based on new concepts: low- or no-selectivity overpolish slurry and stacked pads on a Mirra platform. A second STI CMP process under development uses hard solo pads for significantly improved planarity. A third process, also under development, is based on an advanced slurry and exhibits significantly improved dishing and erosion performance.

Introduction:
STI has been used in volume production for all types of devices from advanced microprocessor to analog to memory devices when the transistor gate width is scaled down to 0.25µm and below. Typically, the percent of active area in analog devices is less than 50%, while the percent of active area in advanced memory devices is greater than 50%. The percent of active area varies from device to device and from site to site within the same device. As a trend, more and more IC manufacturers are exploring mixed-signal-device or system-on-a-chip technologies on their pilot

lines and are starting to implement them in volume production. Both memory and analog portions co-exist on the same chip of a mixed-signal device. As a result, the percent of active area will vary from 10 to 90% in the worst case. The variation of the percent of active area and feature size makes the trench oxide dishing and nitride hard mask erosion difficult to control resulting in device performance failure. The greater the variation, the more negative the impact on device performance. To minimize the dishing/erosion variation, many IC manufacturers use one or more process-integration solutions including reverse mask etch, dummy features, blanket nitride film, and thin nitride film in sandwich. All of these process-integration solutions increase the number of process steps and the manufacturing cost. Some process-integration solutions also have limitation to some device applications. The use of the STI processes reported in this work can eliminate some or all of need for the process-integration solutions.

Experimental:

A Mirra polishing system with patented multi-head and multi-platen architecture, an advanced Titan Head carrier, and an ISRM endpoint detection system was used.(1-3) A modified MIT mask as shown in Figure 1 was used for 8" wafers in this work. On the mask, there are density structures having different percentages of active area (10 to 90%) with fixed pitch (100µm) and test structures of varying trench width.

Results and Discussion:

Production-proven STI CMP process

The first production-proven STI CMP process was developed on a Mirra polishing system.(4) The multi-head and multi-platen architecture provides process flexibility, buffing capability for low defects, and high throughput for low CoO. The ISRM endpoint detection system provides reliable end-pointing and consistently low WIWNU. The advanced Titan Head carrier design with an AEP™ retaining ring and an optimized process provides improved WIWNU and planarity. The Mirra system achieves minimized dishing during over-polishing with a low- or no-selectivity slurry. Typical oxide removal results are presented in Figures 2 and 3 as reported in previous work.(1, 4) The STI CMP process offers repeatable oxide removal and nitride thickness at the same testing features.(4) Dishing performance is presented in Figure 4. The results indicate that dishing at narrower trenches is much less than at wider trenches. Based on the correlation of dishing to trench width, wider trenches were selected for dishing evaluation when developing new STI processes to improve dishing performance. Using the ISRM endpoint detection system, trench oxide dishing can be minimized or eliminated for a specific trench width range while all oxide residues are removed in the active area as shown in Figure 5. The results indicate that this process provides a wider end-pointing-process window on an HDPCVD oxide film than on an SACVD film. The phenomenon is possibly attributed to the hardness of HDPCVD oxide film. However, the ISRM endpoint detection system has been demonstrated to successfully control dishing below 500Å for 400µm trenches, even for an SACVD oxide film as shown by the cross-section SEM and measured step height values both included in Figure 5. This STI CMP process enhanced by ISRM end-pointing has been widely and successfully applied to different devices and different oxide films in volume production.

Hard-solo-pad STI CMP process

An optimized low-pressure process coupled with a hard solo pad is one of two new STI CMP processes under development. As shown in Figures 6 and 7 and Table 1, about 3x planarization efficiency improvement is achieved by using a hard solo pad (IC1000 top pad) at a low pressure (2 psi) as compared to a stacked pad (IC1000-top-pad/Suba IV) at a high pressure (7psi).

Planarization efficiency is evaluated by modeled planarization length, step height range, and trench oxide thickness range. A model to calculate planarization length was developed by the MIT group.(4, 5) Step-height range is calculated by subtracting the smallest step height (10% structure) from the largest step height (90% structure). Similarly, trench oxide thickness range

is calculated by subtracting the smallest trench oxide thickness from the largest trench oxide thickness across 40 to 1000µm wide trenches. Both longer planarization length (up to 15 mm for a hard solo pad) and smaller step height range or trench oxide thickness range represent high planarization efficiency.

Dishing variation is significantly improved by the hard solo pad process as indicated by the trench oxide thickness range across 40 to 1000µm wide trenches after 3000Å oxide film removal (Table 1). The hard solo pad process has demonstrated potential on the Mirra polishing system in a production environment. The process will be further improved with advanced polishing head designs and new pad technology.(6)

Table 1. Normalized step-height range and trench-oxide-thickness range of the hard-solo-pad process (2 psi, IC1000 top pad) compared to a current baseline process (7 psi, IC1000 stacked pad with Suba IV) after 3000Å oxide film removal.*

CMP process type	Normalized step height range**	Normalized trench-oxide thickness range***
Baseline process	1	0.09
Solo pad process	0.4	0.05

* The amount of oxide film removed was measured at a reference feature (the 90% density structure).
** Normalized step-height range is the ratio of actual step height range over reference step-height range when the baseline process was used after 3000Å oxide film removal.
*** Normalized trench-oxide-thickness range is the ratio of actual trench-oxide-thickness range over reference step-height range when the baseline process was used after 3000Å oxide film removal.

Advanced-slurry STI CMP process

Advanced new slurries have been evaluated for improved dishing/erosion performance. These slurries cover the spectra of low and high selectivity, fused and colloidal silica, SiO_2 and CeO_2, and different chemical additives. Among all the slurries evaluated thus far, one showed excellent results in terms of trench oxide dishing and nitride erosion. As compared to the baseline process, the advanced slurry CMP process showed 70% reduction in nitride erosion and 75% reduction in trench oxide dishing. Dishing and erosion performance of the advanced slurry process compared to the other processes is summarized in Table 2.

Table 2. Oxide dishing and nitride erosion reduction of new STI CMP processes under development as compared to the current baseline process.

CMP process type	Nitride erosion reduced	Oxide dishing reduced
Stacked pad at low pressure	30%	42%
Solo pad at low pressure	50%	58%
Advanced slurry	70%	75%

As compared to all the processes evaluated thus far and reported in the literature, the advanced slurry process showed the best oxide dishing and nitride erosion performance. The advanced slurry process showed 40% improvement both in terms of oxide dishing and nitride erosion when compared to the hard solo pad process.

The advanced slurry process has also demonstrated the ability to uniformly remove oxide and minimize nitride erosion across a patterned wafer as shown in Figures 8 and 9. It is important to control uniform oxide film deposition prior to CMP operation for desirable within-wafer non-uniformity (Figure 8). When an ISRM end-pointing system is used with the advanced slurry process, nitride erosion is uniformly minimized across the wafer at the different density structures and features (Figure

9). The nitride erosion value is the difference between pre and post CMP nitride film thickness. In both Figures 8 and 9, the relative film thickness or removal value is the ratio of the actual value over the pre CMP film thickness as deposited.

Conclusion:

Using the Mirra polishing system, low-selectivity-slurry STI CMP has been successfully demonstrated in the volume production of various devices with different oxide films. Two new processes developed on the Mirra CMP system have exhibited improved planarization performance over various features and density structures. Over a range of 10 to 90% active area and 40 to 1000µm trenches, the hard-solo-pad process improved oxide dishing and nitride erosion by at least 50%, and planarity by about 3 folds. The advanced slurry process has demonstrated the further improvement in oxide dishing and nitride erosion performance by at least 70%. The advanced slurry process also exhibited the capability to uniformly remove oxide and minimize nitride erosion across a wafer. Both new processes showed potential as direct STI CMP solutions for advanced IC devices such as mixed-signal devices with varying percent of active area from 10 to 90%.

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	1	2	3	4	5
A	70% Density Structure	60% Density Structure	50% Density Structure	40% Density Structure	30% Density Structure
B	10% Density Structure	90% Density Structure	1.0 μm line/1.0 μm space	20% Density Structure	80% Density Structure
C	HDP-1	0.5 μm by 0.5 μm checker board	Solid Squares / SEM & leg	0.5 μm line/0.5 μm space	2.0 μm line/2.0 μm space
D	HDP-2	1.0 μm by 1.0 μm checker board	2.0 μm line/1.0 μm space	4.0 μm line/1.0 μm space	8.0 μm line/1.0 μm space
E	HDP-3 / ASM wafer global mark	2,4, 10,20 μm Comp. Pitch Structure	40,100,200, 500 μm Comp. Pitch Structure	1000 μm Pitch Structure	2000 μm Pitch Structure

20 mm (width) × 20 mm (height)

Fig. 1. A layout of a modified MIT mask (STIAM).

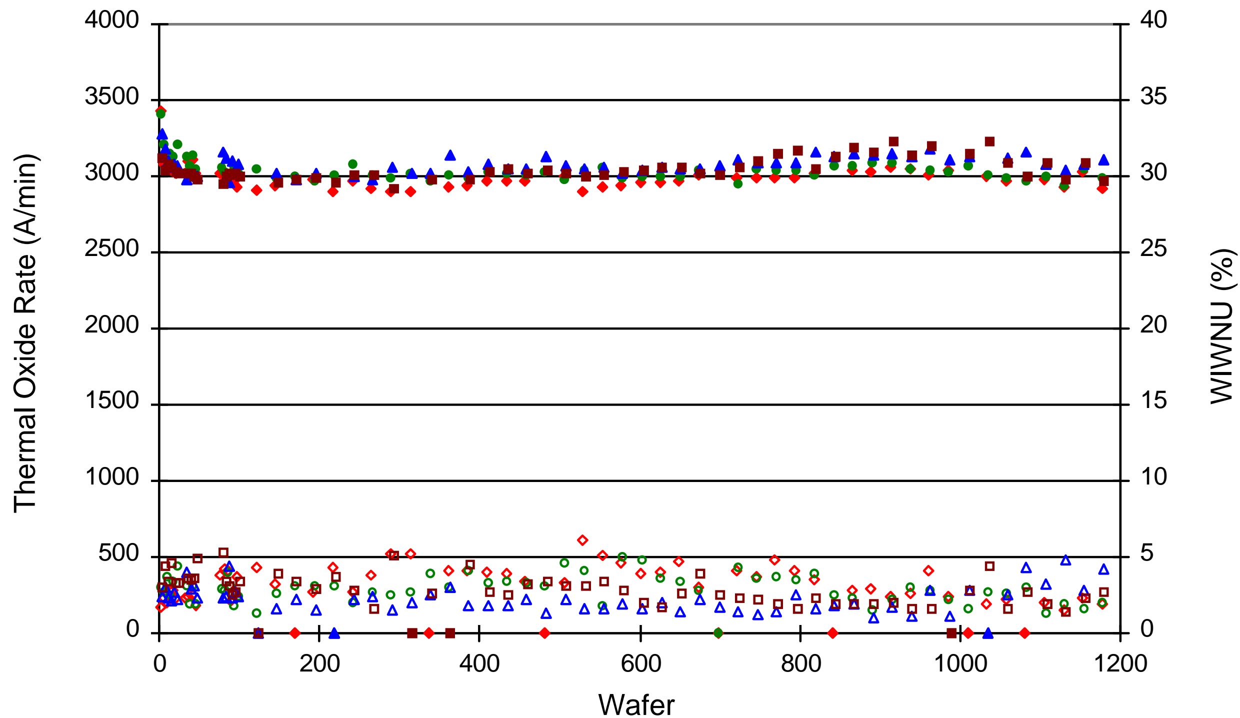


Fig. 2. Oxide removal rate and within wafer non-uniformity at 5 mm edge exclusion as a function of number of wafers polished in an extended run.(1)

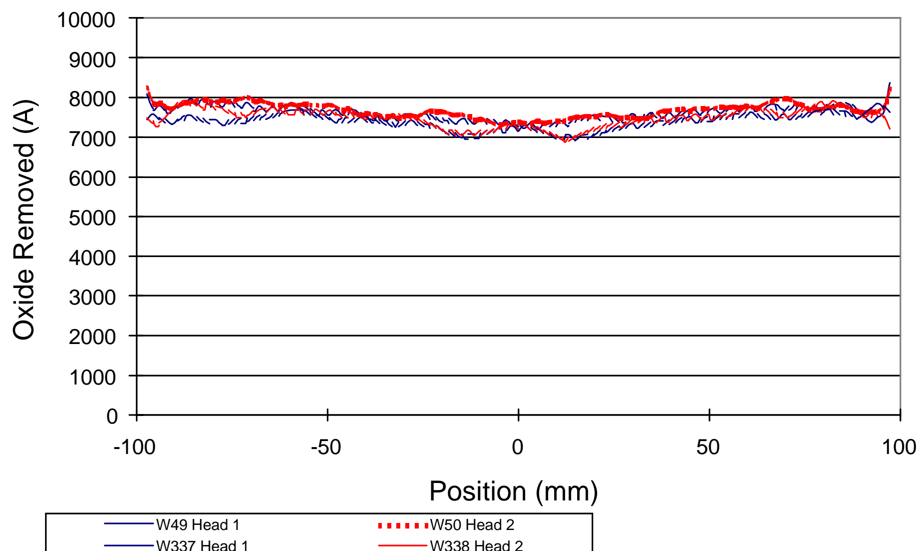


Fig. 3. Wafer diameter scans at 3 mm edge exclusion obtained from different wafers and different polishing heads.(4)

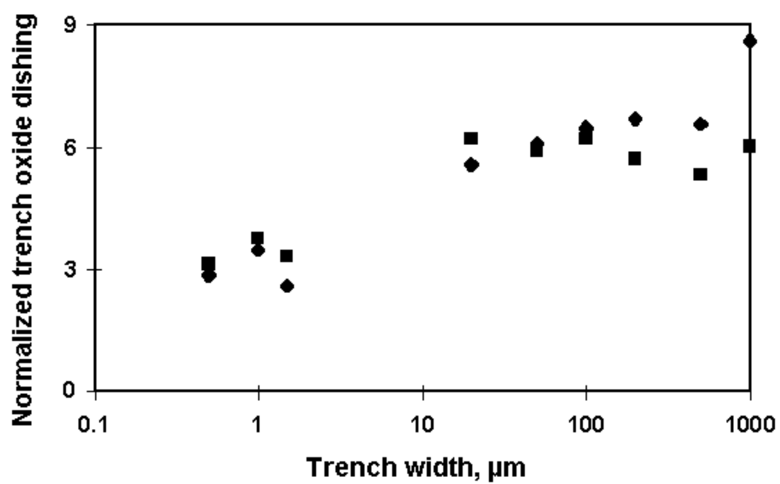
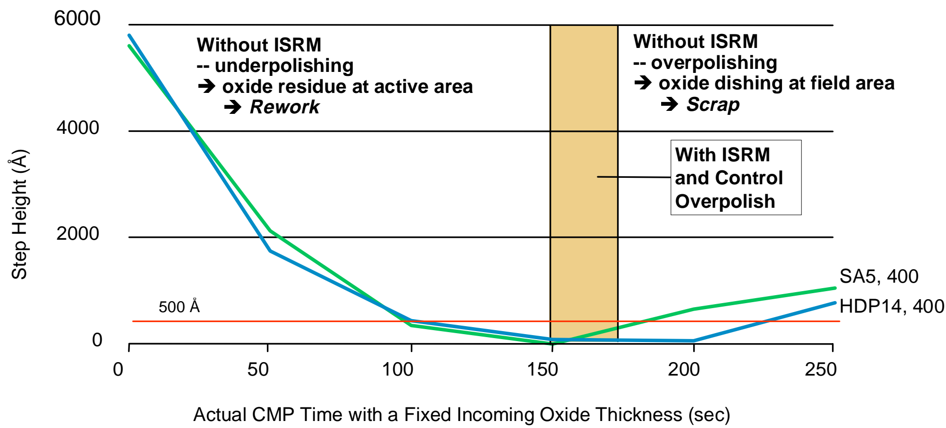
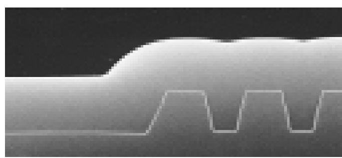


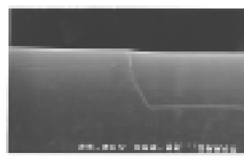
Fig. 4. Trench oxide dishing as a function of trench width.



50% density, 400µm line/space , Giga-fill SACVD & HDPCVD



Prior to STI CMP



After ISRM Endpoint Control

Fig. 5. Step height as a function of polishing time for two different types of oxide films (HDPCVD and SACVD).

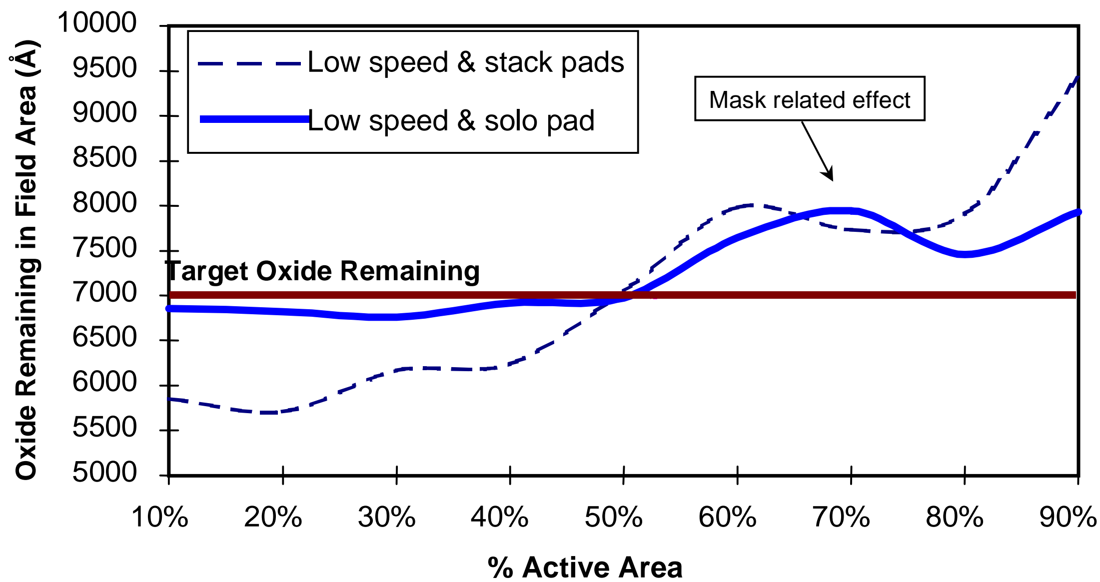


Fig. 6. The impact of pad hardness and polishing pressure on the step height range across 10-90% active area recorded after removing 9000Å oxide at 50% density structure.(4)

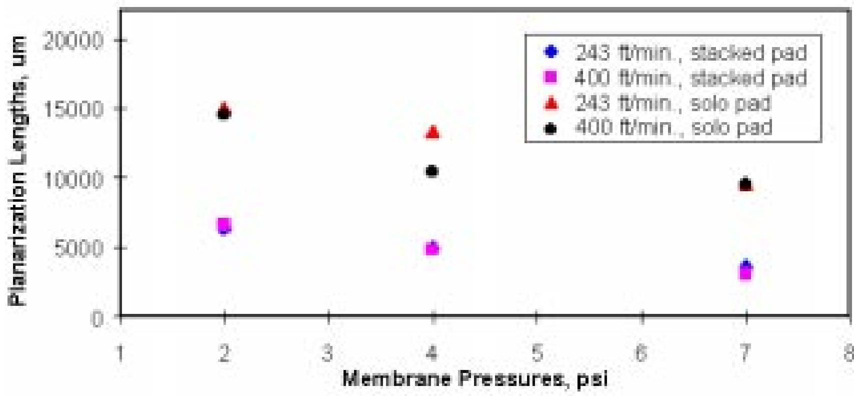


Fig. 7. The impact of pad hardness, polishing pressure, and speed on modeled planarization length.(4)

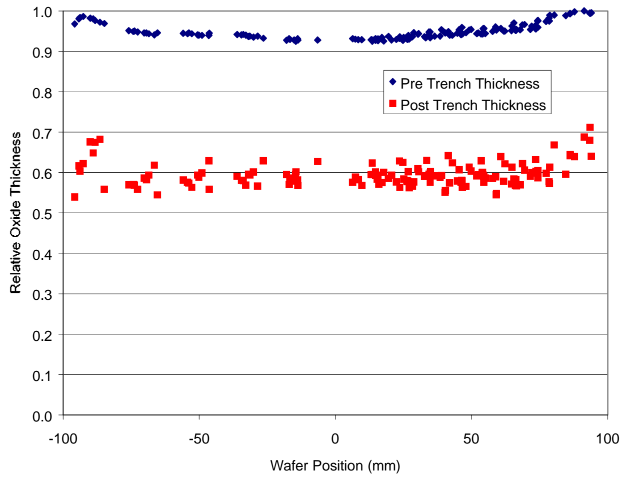


Fig. 8. Trench oxide thickness before and after CMP as a function of the testing site position on a wafer.

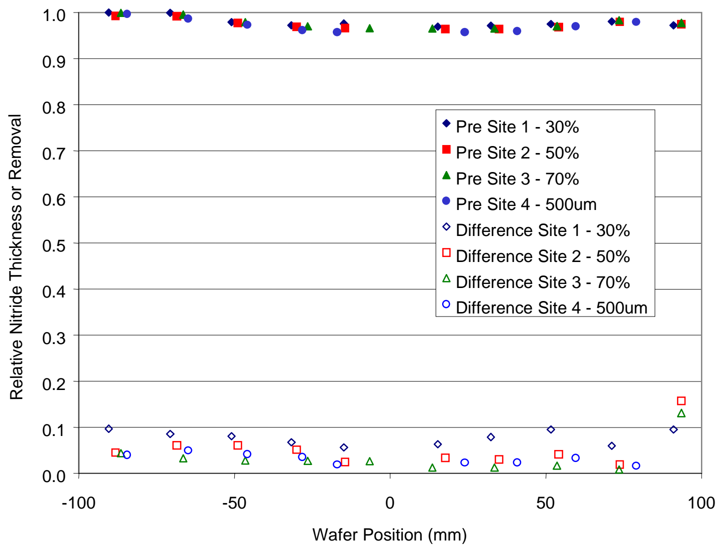


Fig. 9. Nitride erosion at different density structures and features as a function of the testing site position on a wafer.