# Proven Practice and Future Application of Polysilicon CMP in IC Fabrication**

**Raymond R. Jin, Shijian Li, Simon J. Fang*, Fritz Redeker**
**Applied Materials, 3111 Coronado Drive, M/S 1510, Santa Clara, CA 95054**
*** Texas Instruments, 13570 N. Central Expressway, M/S 3701, Dallas, TX 75243**
**(408)986-3277 (phone), (408)235-6803 (fax), raymond_jin@amat.com (e-mail)**

**Biography:**

**Raymond Jin** was an honorary graduate from University of Utah with a Ph.D. in Metallurgy and Materials Science in 1988. He has 10 years of industrial experience as a technologist, program manager, section head/manager in oxide-CMP/STI-CMP/W-CMP/(poly)silicon-CMP, Cu and polymer polishing, new material/chemical R&D, capital equipment selection, and 0.5u/0.35u/0.25u/0.18u/0.15u front/back end CMOS/BiCMOS process module development/integration/transferring. He was credited for a leadership role in improving die yield by 30% in a memory fab and by 40% in an analog/mixed-signal fab. Prior to joining Applied Materials, he worked at National Semiconductor, Cypress Semiconductor and Pilkington. He is currently Global Product Manager mainly for oxide, STI, polysilicon, silicon, low k dielectrics CMP applications and Program Manager for strategic CMP consumables program in the CMP division at Applied Materials. He has 27 technical publications, 17 presentations at technical conferences and 3 patent filings.

**Shijian Li** received his BS degree in Chemistry (majoring in Polymer Science) from Nanjing University, China in 1982 and Ph.D. degree in Chemistry (Spectroscopy and Theoretical Chemistry) from University of Oregon in 1987. He was a research associate in the department of chemistry at Colorado State University and Columbia University before 1992. He joined Applied Materials in 1993 and had experience in both HDP CVD and CMP. He is now a senior member of technical staff in charge of Si, polysilicon and Al CMP processes. He has numerous patents awarded and filed.

**Simon J. Fang** was born in 1967 in Taipei. He received BS degree in Physics from National Central University, in 1989; MS and Ph.D degrees in Materials Science and Engineering from Stanford University in 1993 and 1996, respectively. From 1992 to 1996, he was a research assistant in the Center of Integrated Circuit of Stanford University. His research work included surface characterization, cleaning technologies, and gate oxide integrity. In 1996, he joined Semiconductor Process and Device Center of Texas Instruments, where he was responsible for developing advanced CMP processes and evaluating novel CMP equipment. His current research interests include advanced process control, dielectric and polysilicon CMP, CMP modeling, and interconnect technologies. He has four patents filed, and has authored or co-authored 20 technical papers.

**Fritz Redeker** received his BS degree in Chemical Engineering from the University of California, Berkeley, in 1981. From 1981 through 1987 he was engaged in thin film, etch and hot process development and integration for high speed bipolar and BiCMOS logic and memory devices first at Amdahl Corporation and then at Saratoga Semiconductor. In 1988 he joined Applied Materials, where he has participated and/or driven the development of a variety of etch, dielectric CVD and CMP processes and hardware. He is currently the Director of Technology for CMP division of Applied Materials.

**Abstract:**
This paper reviews and reports advancements in polysilicon CMP development for five different applications in IC fabrication. The most noticeable one is polysilicon plug CMP for DRAM applications. The second is polysilicon gate CMP. The third is dual salicide and self-aligned metal gate (SAMG) formation. The fourth is deep/shallow trench polysilicon CMP for isolation applications. The fifth is sacrificial emitter polysilicon CMP for BiCMOS application. A polysilicon plug CMP process has been developed in Applied Materials' application lab and proven at a customer's DRAM fab on a MIRRA® CMP equipment. A low within wafer non-uniformity (WIWNU, 2.7% 1 sigma at 49 points and 5mm edge exclusion) has been achieved using a best-known-method (BKM) with a stable removal rate of 3625 Å/min. The removal rate can be adjusted in the range of 3000 to 6000 Å/min. without adverse impact on the WIWNU by changing slurry. The BKM consists of oxide breakthrough polish prior to polysilicon main polish followed by polysilicon overpolish. A robust process assisted by reliable endpoint detection has been developed for polysilicon CMP. A new pre-cleaning process including buffing and the surface conversion (from hydrophobic to hydrophilic) has also been developed as a post CMP step of the BKM to achieve a low defect level (25 counts at 0.16u for 8" wafer on Tencor 6200). The polysilicon CMP process is applicable to the polysilicon gate formation. The MIRRA® platform has demonstrated to be the tool of choice for other emerging polysilicon CMP applications (such as dual salicide and self-aligned metal gate formation, deep/shallow trench isolation, and BiCMOS emitter formation) by meeting application requirements.

**Introduction:**
Polysilicon CMP is a preferable process for polysilicon plug formation for high performance DRAM applications.(1) Successful polysilicon CMP is critical for dual salicide and self-aligned metal gate formation.(2) More and more polysilicon/silicon CMP applications are being explored in the R&D facilities of IC manufacturers and gradually becoming a main stream process in mass production for high performance IC devices. This paper will report advancements in polysilicon/silicon CMP development on a MIRRA® platform and review different polysilicon applications in IC fabrication.

**Experimental:**
All polysilicon and silicon CMP experiments as well as the polishing marathons reported in this work were executed on a MIRRA® platform which has been successfully used in oxide (PMD and ILD), shallow trench isolation (STI), and metal (W) CMP in mass production.(3) The MIRRA® platform has also been used in pilot line production for polysilicon CMP and Cu CMP applications and in a R&D for Al CMP applications. The MIRRA® platform is a CMP tool consisting of four heads and three platens where process performance can be independently controlled by varying consumables such as slurries, pads and conditioners, and process parameters (including pressures, rotation speeds) for process flexibility and a potentially wider process window. A new polishing head (Titan Head™) design was used throughout this work. The Titan Head design features a flexible membrane that applies a uniform pressure to the wafer's backside. A new retaining ring with independent pressure control is used to modulate the removal rate at the edge of the wafer to achieve a low non-uniformity. Both 8" and 6" wafers were processed on the tool by changing the heads designed for the wafer size. Both notched and flat wafers were processed using similar hardware settings.

A wide variety of polysilicon/silicon wafers (including un-doped, doped, in-situ doped, RTP annealed, amorphous silicon) were used in this work. The best-known-method (BKM) was applied to all types of polysilicon/silicon wafers:
- both 8" if not specified and 6",

- both notched and flat wafers (with possible minor adjustment).

The wafer types will be specified in the results section as applicable.

Various polyurethane based pads from Rodel were used. Typically, k-grooved IC1000/Suba IV pads were used on platens 1 and 2 for native or cap oxide breakthrough polish using an oxide slurry (on platen 1) and polysilicon or silicon main polish using a silica slurry (platens 1 and 2) while a soft pad was used on platen 3 for buffing with Rodel's Advansil 2000 slurry and rinsing with SC1 cleaning solution ($NH_4OH$:$H_2O_2$:$HO_2$ = 1:4:20). The specific consumable sets for a given application will be described in the results section.

**Results and Discussion:**

Polysilicon/Silicon CMP Characterization

Both polysilicon and amorphous silicon are used for different polysilicon applications in IC fabrication. Amorphous silicon is generally viewed to be easier to be processed in the fab as compared to polysilicon which consists of numerous polysilicon grains of different sizes depending on the doping/annealling level. In the case of doped/annealed polysilicon, the dopant (such as P) will be concentrated along the grain boundary creating a heterogenous phase. In the case of highly doped polysilicon, prevention of dopant escape by using a cap oxide layer or other means is always of importance to process integration. In these regards, amorphous silicon CMP has been integrated in IC fabrication although added doping/annealling steps to convert amorphous silicon to polysilicon after CMP may increase cost of ownership as compared to in-situ doped polysilicon CMP. Amorphous silicon CMP is chosen in some fabs partially due to more technical challenges in the process control of in-situ doped polysilicon film deposition. Because of the importance of amorphous silicon CMP in IC fabrication, amorphous silicon CMP was conducted along with polysilicon CMP in our characterization.

*Removal rate, non-uniformity, and selectivity*

It is critical to remove the native or cap oxide layer before polysilicon main polish using high selectivity (polisilicon:oxide) slurries in order to achieve a low WIWNU. Without proper removal of the native or cap oxide layer, the WIWNU can be as high as 38.4% as shown in Table 1. The WIWNU is reduced to 3.04% or less by removing the native or cap oxide layer in a oxide breakthrough polish step while maintaining a stable high removal rate of about 3200 Å/min. In this regard, a process flow as shown in Fig. 1 was employed in the BKM process to ensure a low WIWNU and a consistent removal rate. Post CMP oxidation using $H_2O_2$ was carried out to prevent the dopant escape for doped polysilicon, to convert the hydrophobic surface to hydrophilic, and to perserve the post CMP polysilicon surface quality. Polysilicon overpolish was added after polysilicon main polish to ensure complete polysilicon removal in the unwanted area. The oxide breakthrough polish time can be changed depending on the thickness of native oxide (on the order of 10 to 20 Å) or cap oxide (in the range of 100 to 400 Å). Applying inadquate and fixed oxide breakthrough polish time to the wafers of different oxide thickness will result in a significant polysilicon main polish removal rate change.

Table 1. The impact of oxide breakthrough polish (OBTP) on the polysilicon removal rate and WIWNU.

| Process | Wf. # | Removal Rate, A/min. | WIWNU, % |
|---|---|---|---|
| Without OBTP | 1 | 1100 | 24.6 |
| Without OBTP | 2 | 66 | 38.4 |
| With OBTP | 3 | 3209 | 2.4 |
| With OBTP | 4 | 3294 | 3.0 |

The selectivity of amorphous silicon or polysilicon over thermal oxide for the slurry used in the main polish step is in the range of 100-220:1. The selectivity of amorphous silicon or polysilicon over thermal oxide for the slurry used in the buffing step is 1:1. The selectivity of thermal oxide over amorphous silicon or

polysilicon for the slurry used in the oxide breakthrough polish step is also 1:1.

*Polish endpointing*

To control the post CMP silicon film thickness, an in situ rate monitor (ISRM$^{TM}$) system was used. As shown in Fig. 2, the ISRM$^{TM}$ system is a non-contact and laser-based device. It detects the endpoint of polysilicon/silicon polish by measuring the relative thickness changes of polysilicon or silicon film layers and stops polishing when the required amount of the film is removed or a stopping layer is reached. The ISRM$^{TM}$ system records the optical signal which correlates to the change of thickness of the film being polished. An optical signal pattern recognition algorithm ensures successful endpoint detection after processing the optical signals which exhibit reproducibility for a given type of wafer. To test the ISRM$^{TM}$ system capability, the post CMP fim thickness and actual end point time were evaluated without pad break-in by diamond disk. The results are plotted in Figs. 3 & 4. The results showed that without standard pad break-in as used in the BKM, it took 21 break-in wafers to eliminate the actual endpoint time variability. This variability was mainly due to the polishing removal rate variability as caused mainly by pad temperature fluctuation. However, the ISRM$^{TM}$ system ensured the post CMP film thickness consistentcy even during the wafer break-in period with exception of the first wafer which was used for developing the ISRM$^{TM}$ endpoint algorithium.

As shown in Fig. 3, a stable removal rate of 590 to 666 Å/min at a non-uniformity of less than 4% can be achieved for the 8" wafers after pad break-in. In this application for final polish using slurry A (a fumed silica based slurry), the non-BKM soft pad for silicon main polish is not grooved or embossed and not conditioned in-situ or ex-situ using diamond disk to achieve the finest surface quality, low non-uniformity and low removal rate as desired by a customer. When the process was applied to 6" wafers of the same type, tight process control was also achieved with the average WIWNU of 2.78% at 5 mm edge exclusion.

*Head to head matching*

Head to head matching was also evaluated to ensure tight process control. Four different heads were used for evaluation in terms of average post CMP within wafer non-uniformity at 3mm edge exclusion, and the average final film thickness when the ISRM$^{TM}$ system was used in an extended run. The results are summarized in Table 2.

Table 2. Head to head matching in terms of average post CMP within wafer non-uniformity and range at 3mm edge exclusion, and the average final film thickness and standard deviation.

| Heads | #1 | #2 | #3 | #4 |
|---|---|---|---|---|
| Ave. WIWNU, % | 2.42 | 2.40 | 2.17 | 2.20 |
| Ave. Range, Å | 143 | 146 | 129 | 132 |
| Ave. thickness, Å | 2091 | 2079 | 2076 | 2087 |
| Ave. standard dev., Å | 51 | 50 | 45 | 46 |

The results showed that four different heads matched well during the extended polish run.

*Post CMP cleaning*

The post CMP defects were characterized using Tencor 6200 at >0.16 microns. It was discovered that an optimized pre-cleaning process consisting of the buffing using a proper slurry followed by the conversion of the hydrophobic polysilicon or silicon surface to hydrophilic using a proper solution is critical to ensure a low defect count. The typical post CMP results achieved in the application lab of Applied Materials are presented in Fig. 5. The results showed that the optimized post CMP cleaning process ensured the low defect counts (average of 25) at the size of >0.16 microns. Better defect counts have been observed at the manufacturing settings in a production fab.

*Mini-marathon run*

A mini-marathon (i.e., extended) run was executed on undoped polysilicon wafers using the

BKM process described in the experimental section. The results are plotted in Fig. 6. The results showed that a stable polysilicon removal rate and a low WIWNU can be achieved using the BKM process. The average removal rate is 3609 Å/min. based on a 49-point contour map. The average WIWNU is 2.70% at 5 mm edge exclusion based on a 49-point contour map.

The low post CMP WIWNU of an undoped polysilicon film was confirmed by a wafer scan as shown in Fig. 7.

Polysilicon CMP Applications

*Polysilicon plug for DRAM*

Polysilicon plug formation is an important process module in the 1 Gb DRAM technology node (i.e., storage cell). Polysilicon over the field area has to be removed following polysilicon deposition to fill the vias. Reactive ion etch (RIE) has been used for the purpose. However, RIE causes excess dishing in the tiny polysilicon plug. The dishing is magnified due to the recess of the polysilicon film right above the via on the incoming wafers. Even highly selective and anisotropic polysilicon etch will not minimize the polysilicon recess created at the polysilicon deposition step. The extent of polysilicon recess will vary across the wafer due to the change in via size and depth and the non-uniformity of deposited polysilicon film. The varying degree of polysilicon plug recess will cause problems for the barrier layer deposition in the following step and ultimately have adverse impact on the device reliability. To solve the RIE problems, polysilicon CMP has been utilized.

In this work, in-situ P doped polysilicon (both sheet and patterned) wafers were used. The patterned wafers were prepared by depositing the polysilicon film over vias of less than 0.15 microns in diameter. The wafers were used for building test devices for 1 Gb DRAM applications. The polysilicon CMP process performed in this work was considered to be one of the steps to complete production of two full-loop lots. A split of slurry B vs. slurry C for polysilicon main polish was executed for both lots. Both slurries are fumed-silica based. They are formulated by two different supplies. One of the known difference is that the solid/liquid ratio is higher for slurry B than slurry C when dispensed to the platens.

To confirm the importance of native or cap oxide breakthrough polish (OBTP), a mini-split of with vs. without OBTP was conducted on the both main splits of slurry B and slurry C. The results are summarized in Table 3. The results showed that OBTP was important to achieve a low WIWNU. Based on these results, the BKM process with OBTP was used for both splits in both lots: slurry B vs. slurry C. ISRM™ end pointing was successful for all the wafers in both lots. The post CMP defect counts showed similar performance as in Fig. 5 and met customer requirements. The post CMP wafers were examined under atomic force microscope (AFM) and no particles of larger than 1 micron were found at the polysilicon plug surface. Polysilicon plug dishing or recess was found to meet customer requirements by a large margin. The polysilicon CMP performance for polysilicon plug formation reported in this paper has been successfully repeated at customer sites in production settings.

TXRF elemental analyses were conducted on 7 wafers sampled from two lots to ensure no potassium contamination on the device wafers before sending the wafers to next step on the production line. Among the analyzed-elements are K, Ca, Fe, Ni, Cu, Zn, W, P, As, S, Cl, and Si. Nine sites evenly scattered over each wafer were sampled. Only 2 out of 63 sites on 7 wafers showed K at the border line of the analytical instrument detection limit of 2.00E+11 atoms/cm$^2$. The rest of the sites were below the detection limit. The post CMP cleaning in the BKM is shown to be effective to prevent potassium contamination. All elements detected are considered to be normal and acceptable for device wafers on the production line.

Table 3. The impact of oxide breakthrough polish (OBTP) on the wafer-averaged removal rate and WIWNU of in-situ depoed polysilicon.

| Process | Average Removal Rate, A/min. | Average WIWNU, % |
|---|---|---|
| At Applied Materials' application lab: | | |
| Without OBTP, slurry B | 5276 | 9.75 |
| Without OBTP, slurry C | 3511 | 14.3 |
| With OBTP, slurry B | 5204 | 6.01* |
| With OBTP, slurry C | 4019 | 7.20* |
| At a customer's fab: | | |
| Without OBTP, slurry B | - | 10.6 |
| With OBTP, slurry B | - | 3.38* |

* The WIWNU with OBTP was lowered to less than 4% by optimizing OBTP time as showed at a customer's fab.

Amorphous silicon wafers (both sheet and patterned) were also used in this work for high performance DRAM applications. The results are summarized in Fig. 8. An average polishing removal rate of 3000 Å/min. desired by a customer was achieved at a low average WIWNU of 3.64%. All the post CMP pattern wafers were inspected under scanning electron microscope (SEM) at a customer's fab. No residues were found on the surfaces of polysilicon and oxide. The post CMP pattern wafers were also inspected for polysilicon plug dishing and oxide erosion. The results sampled at the 0.3 micron polysilicon plugs across each wafer showed that dishing is less than 200 Å and erosion is less than 500 Å by a significant margin. The results confirmed that polysilicon CMP on a MIRRA® platform meets customer requirements.

*Other polysilicon CMP applications*

Polysilicon gate CMP has been integrated into the deep sub-half micron device manufacturing. Polysilicon gate CMP is expected to improve both photolithography process margins and gate critical dimension (CD) control by planarization and to improve silicide/salicide process margins by smoothing the polysilicon grains and improving polysilicon film surface quality.

Polysilicon CMP has been employed as a key process step for dual salicide and self-aligned metal gate (SAMG) formation for sub-0.25 micron CMOS technologies.(2) Traditionally, polycide ($WSi_x$/ poly) and salicide (commonly, $TiSi_2$ or $CoSi_2$/poly) are used to lower the gate sheet resistance. However, the sheet resistance increases rapidly with decreasing polysilicon CD (<0.40 microns) for salicide. Polycide has its own issues of incompatibility with dual polysilicon CMOS architecture and relative high sheet resistance (10-20 ohm/sq). SAMG Cloisonne process involves the oxide gap fill of the frontend device topography, followed by oxide and polysilicon CMP to planarize the wafer surface and expose the polysilicon patterns. The polysilicon patterns are then partially etched away using high selectivity (>40:1, polysilicon: oxide) etch chemistry to create gate trenches to be filled later by W/TiN or Al/TiN. SAMGs are formed by removing the excess metal using metal CMP at the last step in the process (see Fig. 9). Standard backend processes are used after SAMG Cloisonne process. The metal gates are not subjected to high temperature cycles, as opposed to conventional gate metallization process. SAMG Cloisonne process enables decoupling of gate silicidation from silicon silicidation in the source/drain area which is completed prior to SAMG Cloisonne process steps. Decoupling two silicidation steps (i.e., dual silicide) made low gate resistance possible. Low gate sheet resistance of less than 1 ohm/sq can be easily achieved using the SAMG Cloisonne process. The process is attractive for sub-0.18 micron CMOS technologies. The feasibility of this new process has been shown on working devices.

The deep or shallow trench polysilicon CMP is an alternative to the polysilicon etch back to create reliable transistor-level isolation using undoped polysilicon as an effective dielectric. As compared to etch back, CMP could improve the polysilicon recess uniformity across the wafer and eliminate any potential plasma damage during etch back.

The sacrificial emitter polysilicon CMP could be a novel approach to improve BiCMOS process control by eliminating the topography of polysilicon film retained or worsened during the typically isotropic polysilicon etch back. The uniform polysilicon thickness in the emitter area

could lead to improved device performance due to controlled implant in extrinsic regions and no implant in intrinsic regions. The approach could also reduce the deposited polysilicon thickness and improve polysilicon deposition tool throughput.

*Polysilicon CMP challenges and solutions*

Major CMP-related requirements for success polysilicon CMP applications (such as polysilicon plug formation, conventional polysilicon gate formation, SAMG Cloisonne process, deep/shallow trench isolation, and BiCMOS emitter formation) are

- reliable endpoint to precisely stop after a certain amount of polysilicon has been removed or when the dielectric (such as oxide) stopping layer is reached,
- low WIWNU to ensure the remaining oxide and polysilicon thickness uniform across the wafer,
- high planarity and minimum polysilicon or oxide dishing,
- low defect/scratch counts
- negligible dopant escape for doped polysilicon.

Conventional CMP tools have their technological limitation to meet these requirements. As a new generation CMP equipment, the MIRRA® platform has demonstrated its capability of meeting these requirements as documented in this paper and elsewhere. (3-5)

**Conclusion:**

A polysilcon CMP BKM has been developed on a MIRRA® platform. The BKM consists of oxide breakthrough polish prior to polysilicon main polish followed by polysilicon overpolish. A low non-uniformity (2.7% 1 sigma at 49 points and 5mm edge exclusion) has been achieved in an extended run using the BKM at a stable removal rate of 3625 Å/min. The removal rate can be adjusted in the range of 3000 to 6000 Å/min. without adverse impact on the WIWNU by using different slurry. A low WIWNU is ensured by using a novel oxide breakthrough polish process, a new polishing head design (Titan Head design with a new retaining ring), and a new pad conditioner/disk design. A robust polysilicon CMP process assisted by a reliable ISRM™ endpoint detection system has been developed for different types of polysilicon films. A new pre-cleaning process including buffing and the surface conversion (from hydrophobic to hydrophilic) has also been developed as a post CMP step of the BKM to achieve a low defect level (25 counts at 0.16u for 8” wafer on Tencor 6200). The potential to achieve high planarity and minimum polysilicon or oxide dishing has been shown by process optimization using non-selectivity slurry and low pressure. A thin oxide film is formed during post CMP $H_2O_2$-based SC1 pre-clean to prevent dopant escape. Process flexibility of multiple heads and platens enhances controllability of the novel processes for a low WIWNU, low defects, minimum dishing, and reliable post CMP oxidation.

The MIRRA® platform is capable of meeting the requirements for different polysilicon CMP applications. Polysilicon CMP on a MIRRA® platform is proven in production for both DRAM polysilicon plug formation and polysilicon gate formation. Successful polysilicon/silicon CMP has been demonstrated on different polysilicon/silicon types (undoped, doped, P doped, in-situ doped, RTP annealed, amorphous silicon) and different wafer types (8”, 6”, notched, and flat). The MIRRA® platform has the potential to be the tool of choice for other emerging polysilicon CMP applications (such as SAMG Cloisonne process, deep/shallow trench isolation, and BiCMOS emitter formation) by meeting their requirements.

**References:**

1. S. J. Fang, et al., Proceedings of 1998 CMP-MIC, pp.134-141.
2. M. Weling and X. Lin, The 193rd meeting of ECS, May 3-8, 1998, Abstract #446.
3. R. Jin, “New Generation CMP Equipment and its Impact on IC Devices”, Proceeding of 5th International Conference on Solid-State and Integrated-Circuit Technology, October 21-23, 1998, Beijing, China, in press.

4. D. Chan, et al, “Process Control and Monitoring with Laser Interferometry Based Endpoint Detection in Chemical Mechanical Planarization”, Proceedings of 98 ASMC, in press.
5. R. Jin, et al, Proceedings of 1998 VMIC Conference, pp. 527-529.

**Acknowledgments:**

Among many contributors to this work are Bob Abbassi, Ramin Emami, Satyasrayan Kumaraswamy, Srinivas Satya, Andy Barda, Robert Tolles, Henry Byorum.

---

** This paper has been published in the proceedings of IC Seminar at SEMICON TAIWAN, Taipei, Taiwan, Nov. 4-6, 1998, pp. 263-274.

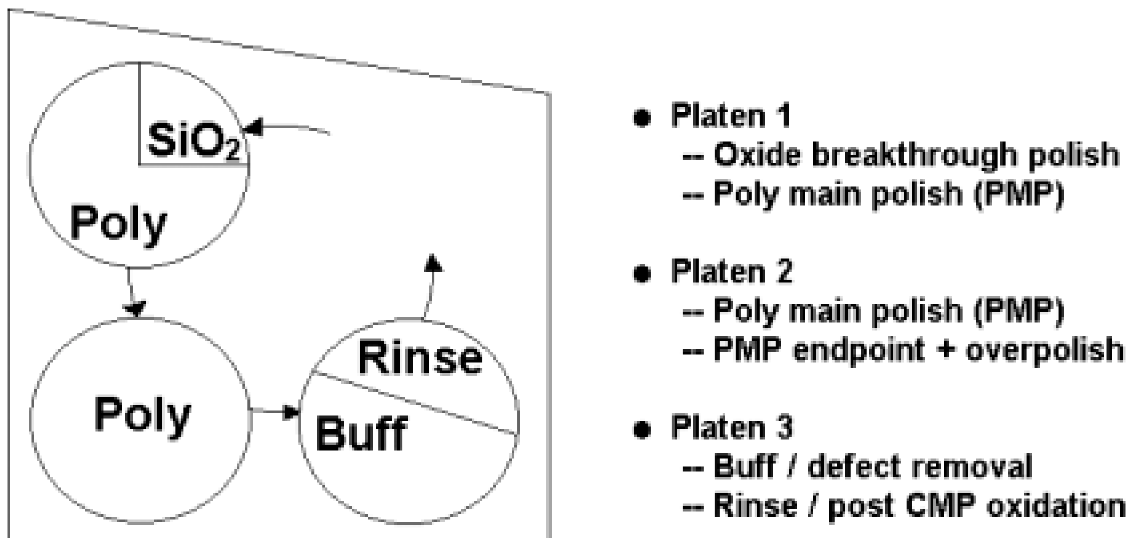


Fig. 1. A polysilicon CMP BKM process flow on a MIRRA® platform.

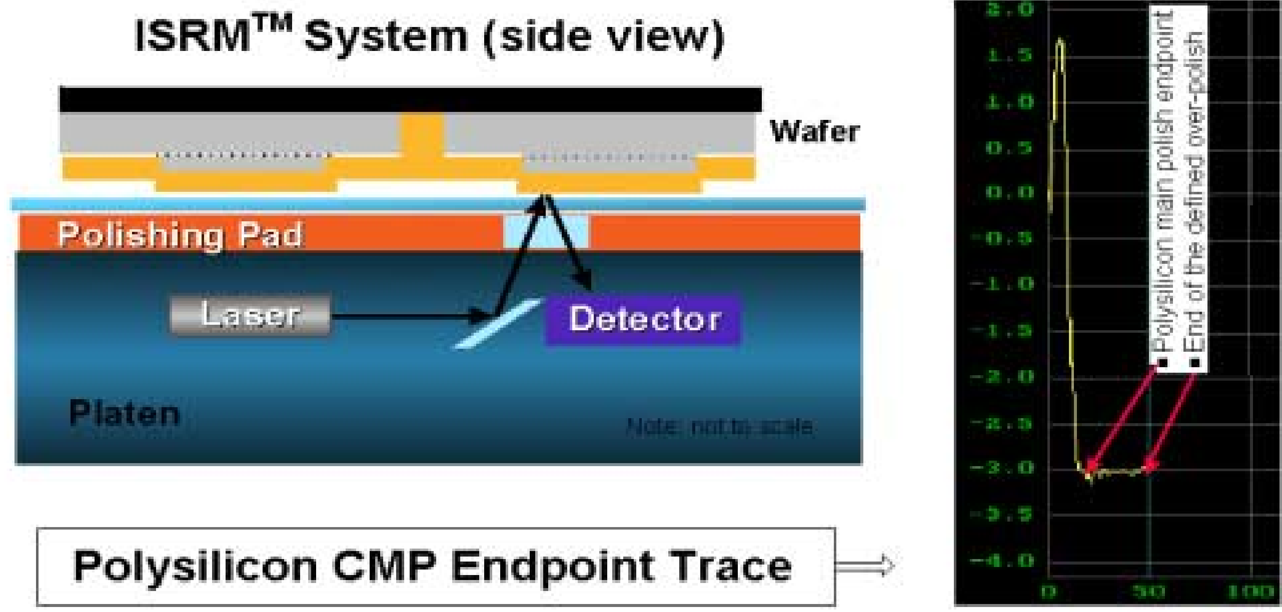


Fig. 2. An in situ rate monitor (ISRM™) system (side view) and a typical end point trace for polysilicon or amorphous silicon polish showing the endpoint of main polish and a defined over-polish.

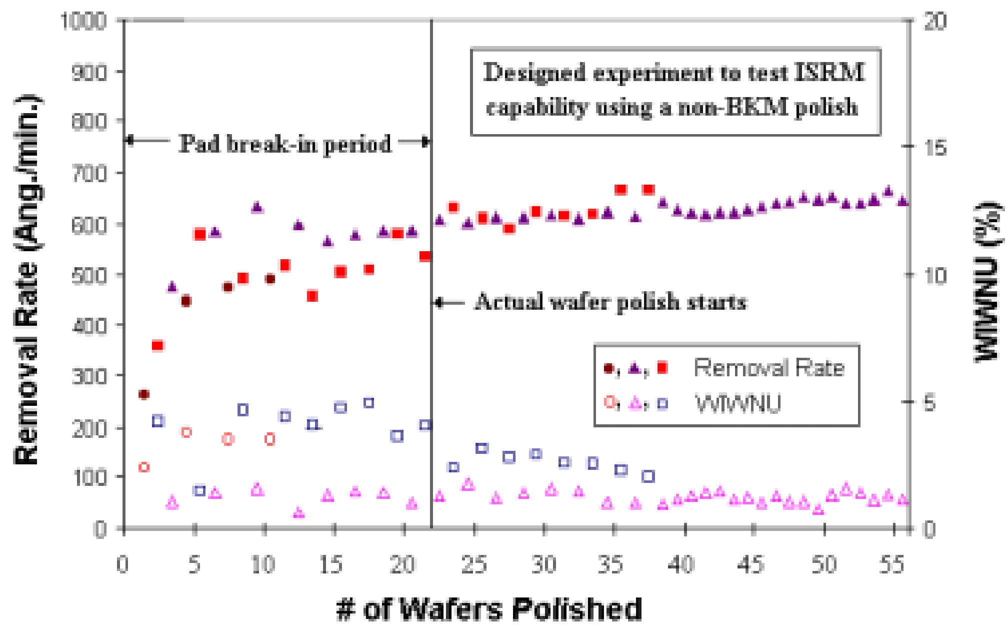


Fig. 3. Silicon polishing removal rate and within wafer non-uniformity at 5 mm edge exclusion as a function of the number of wafers polished without pad break-in using diamond disk.

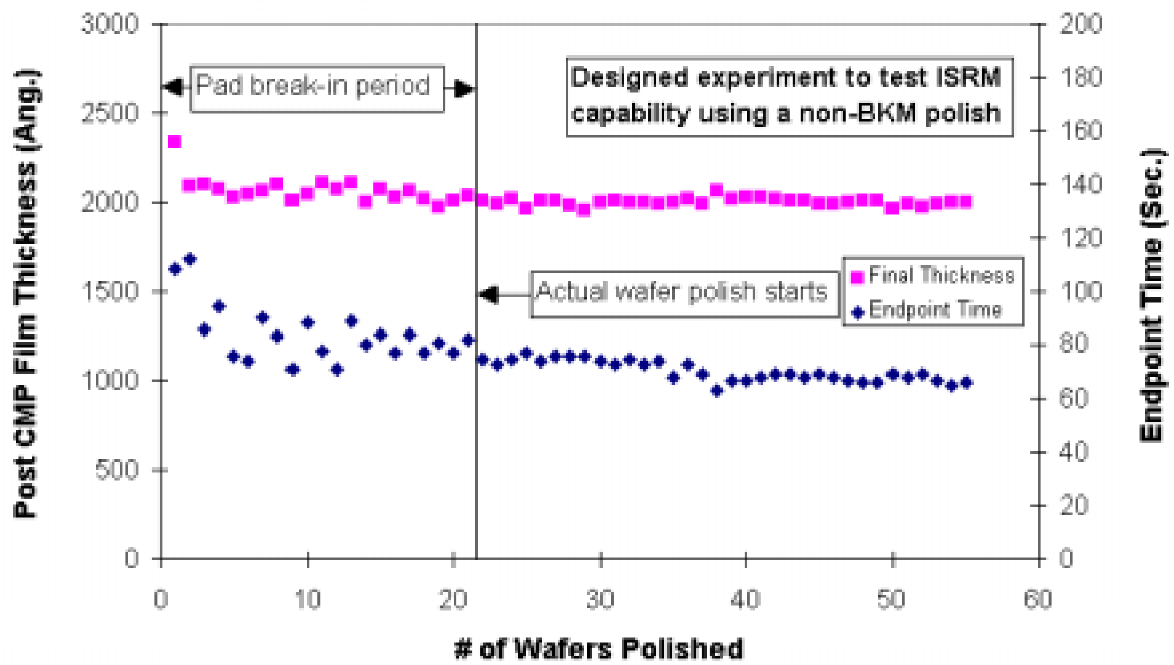


Fig. 4. Post CMP silicon film thickness and silicon CMP end point time as a function of the number of wafers polished without pad break-in using diamond disk.

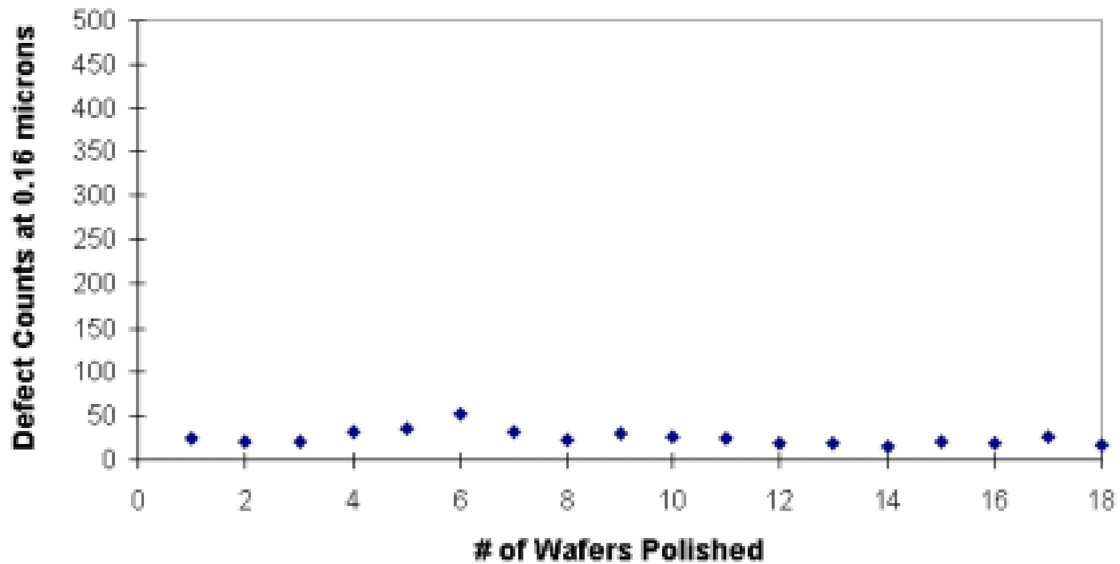


Fig. 5. Tencor 6200 defect counts at 0.16 microns as a function of the number of wafers processed using an optimized post CMP cleaning process.

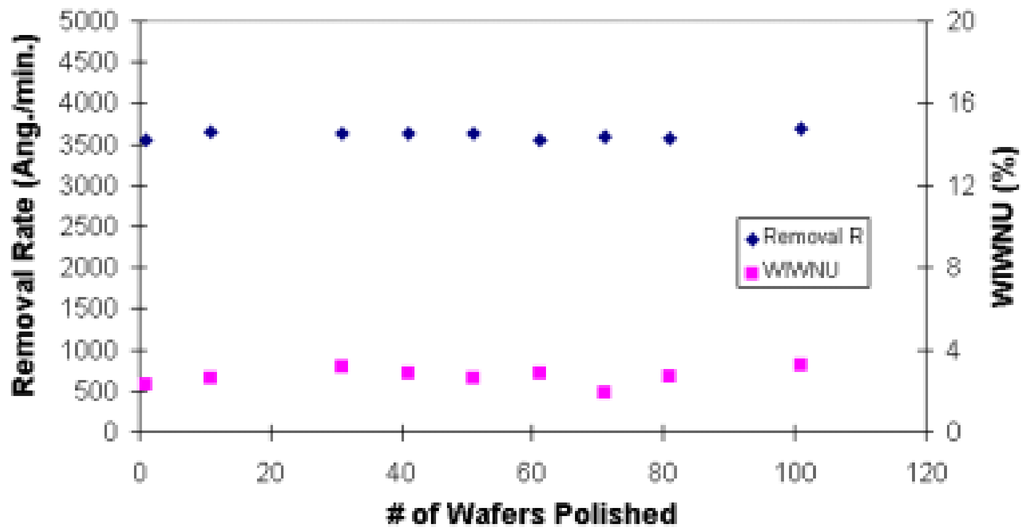


Fig. 6. A mini-marathon run on in-situ doped polysilicon wafers using the BKM process on a MIRRA® platform.

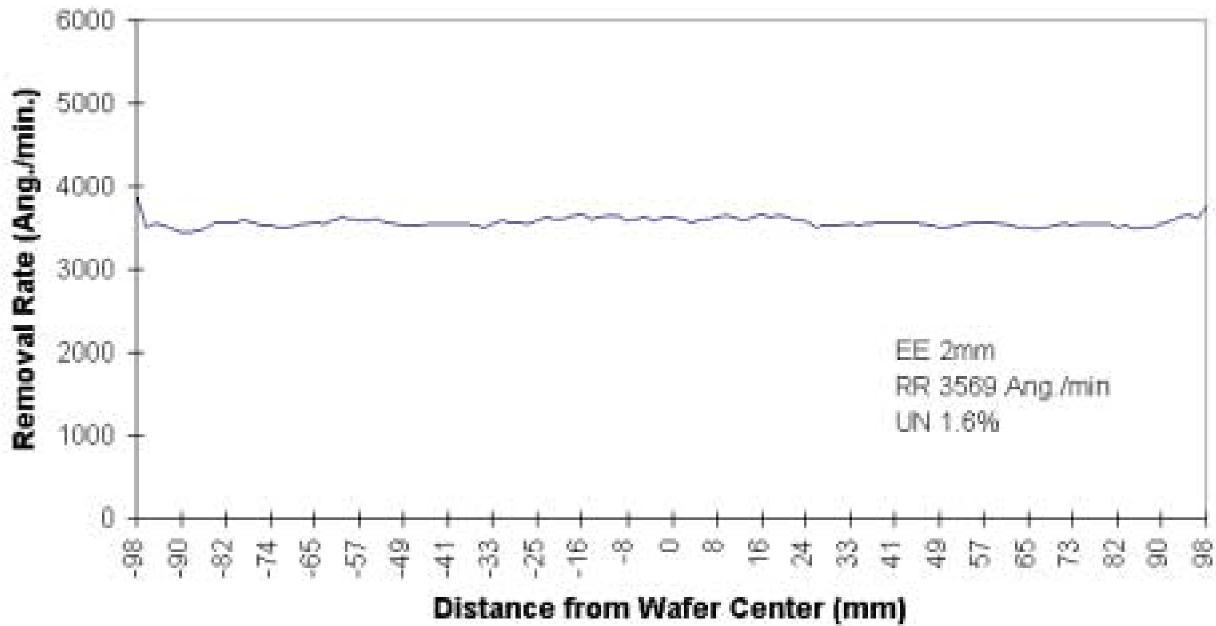


Fig. 7. Post CMP wafer scan for an undoped polysilicon wafer.

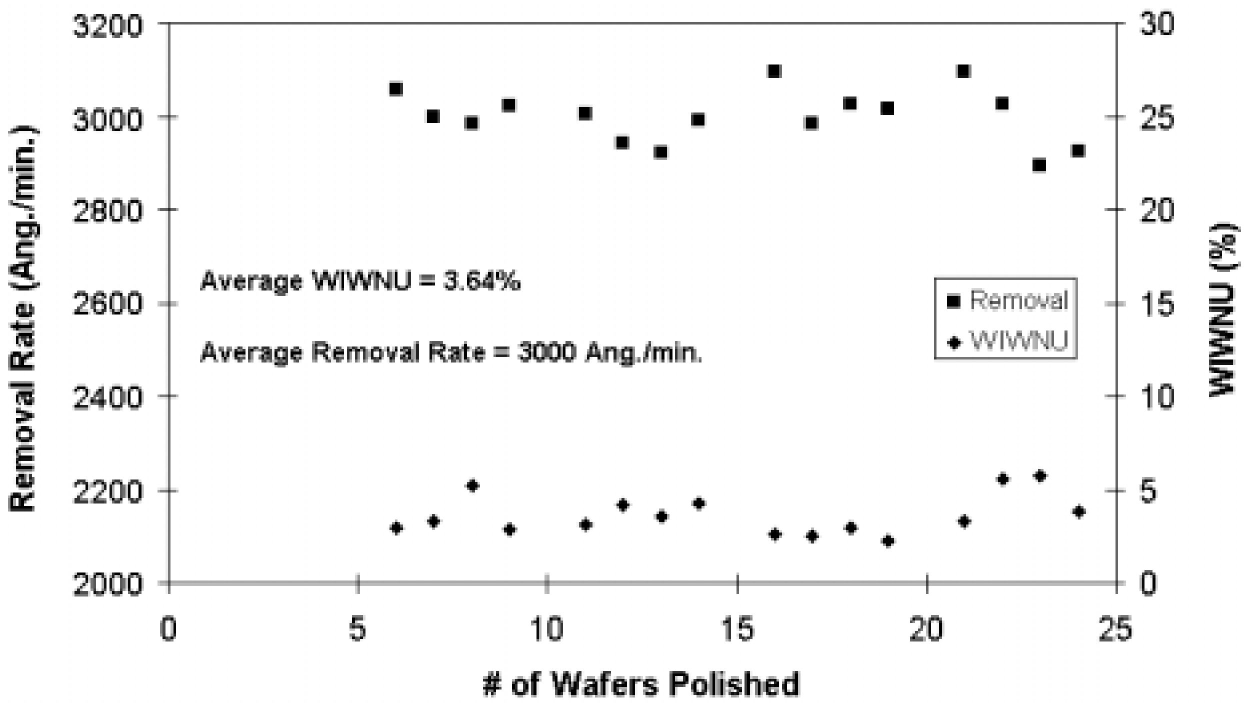


Fig. 8. Undoped amorphous silicon polishing removal rate and within wafer non-uniformity at 5 mm edge exclusion as a function of the number of wafers polished.

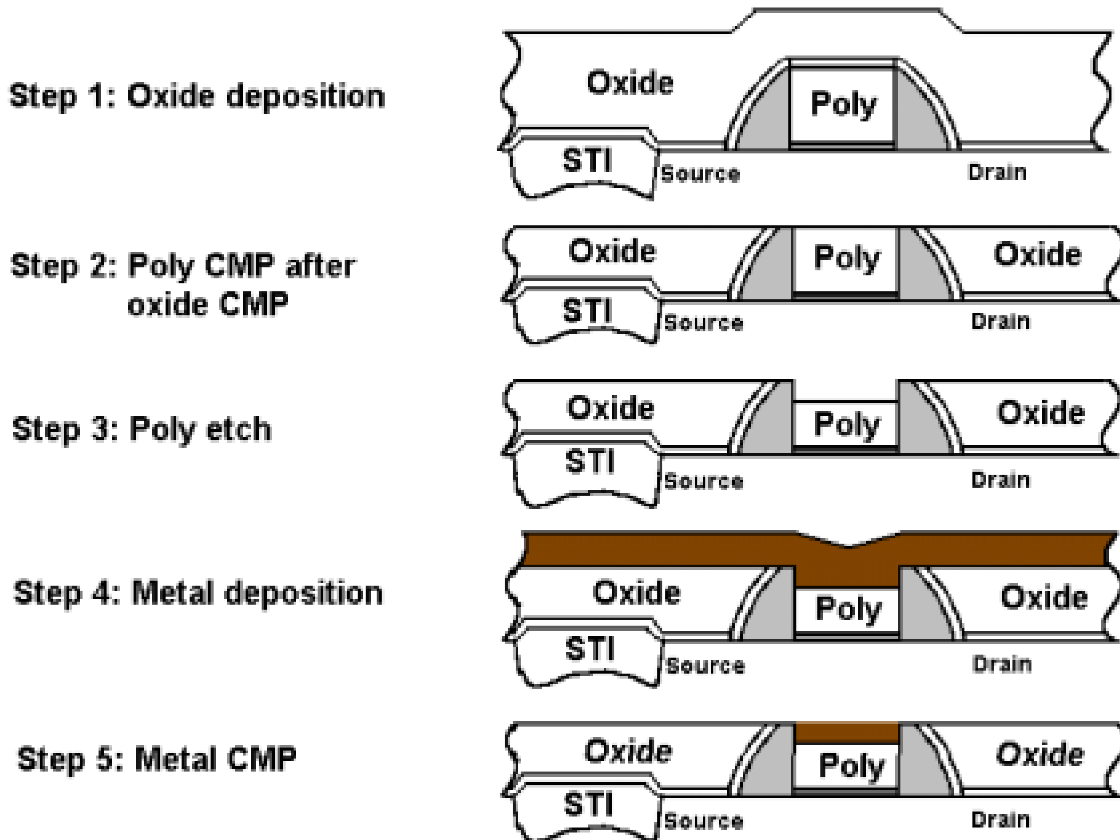


Fig. 9. A schematic diagram of self alligned metal gate (SAMG) Cloisonne process.